# COPLANAR WAVEGUIDE RESONATOR TOWARD SUPERCONDUCTING QUBITS: DESIGN AND FABRICATION

**Treball Final de Grau en Nanociència i Nanotecnologia**

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CSIC Spanish Council of Research

UAB Universitat Autònoma de Barcelona

CNM Centre Nacional de Microelectrònica IMB

## Contents

## 1. Context and motivation of this research work

In a short time period, from the 20th century to the present, modern computers have completely changed the World. The birth of universal computation can be dated to the late 1930s, when mathematician Alan Turing described a theoretical model, that later became known as the Turing machine, by which any calculable function could be actually solved. Several decades later, very important advances in Turing's ideas, their practical realization and an exponential sophistication of the machines have been achieved, so as to reach the impressive capabilities of the actual modern computers that we use in a daily basis, not to mention state of art supercomputers.

Yet, his foundational ideas are still the basis of nowadays computers.

Our classical computers are built upon the concept of bits and digital logic [22]. A bit is the basic element we use to code information and it can take on one of two distinct values, typically labelled as 0 or 1. In physical computers, this concept is implemented by a kind of solid states devices, the transistors, which in operation can take two states, ON or OFF. Based on this, transistors are used to represent, respectively, the 1 or 0 bit state. A computer encodes any information as a series of bits and performs complex operations with them by using dedicated electronic circuits, the so-called logic gates. Logic gates apply a series of simple given rules to each bit, combined and once the operations are finished, the information regarding the result can be decoded from the output bits. Traditionally, a most important characteristic of a computer is how fast it can perform the calculations. In this regard, its computing power is strongly determined by its processor, which defines how many operations can be carried out on a certain number of bits in a given time interval. Additionally, the processor is made of lots of transistors, interconnected, but there are size limitations and circuit design rules, so, for instance, cannot fabricate a processor with an infinite number of transistors. Therefore, with a finite number of transistors, the number of processable bits is also limited, so is the number of calculations that can be made in a time interval. Even if companies like Intel are producing transistors in the 14nm node [26], nowadays, we are not only reaching transistor size limits, but complexity and amount of data is challenging the classical computation. At this point, what is about beyond or future computation?

Actually, in 1981, Richard Feynman [10] proposed to overcome those limitations and problems by a new technology. He proposed mapping the system in quantum bits (in short qubits), where two-level energy system is referred to a quantum system. Particles that can exist in any quantum superposition of those two independent quantum states. In the course of that decade, this idea was further developed, culminating in the concept of the universal quantum computer as follows. Similar to classical bits, the qubit can be in the two values, 0 and 1, as well, but it can also be in any state between those, which form a continuum of superposition of quantum states. Like in the case of classical bits, quantum computing would be operated by gates, quantum gates, to perform the operations on qubits. Also analogously, circuits can be purposely designed to carry out operations on families of qubits, which can also be entangled [3]. Consequently, quantum logic gates can perform a different variety of operations on qubits, and more importantly result in a wider range of inputs and outputs. The change is so important that operations that would take trillion-years on a classical computer could take days or hours if done by quantum processors.

In 2019, quantum computing is still in its infancy. Yet, an important amount of research effort and investment is currently dedicated to advance this technology. Recently, Rigetti Computing from US announced its 128 qubit quantum computer. Nonetheless, the European Comission has begun a coordinated research initiative, called Quantum Flagship, with more than one billion euros invested, following some earlier National initiatives. As stated in its webpage, the purpose is to "*consolidate and expand European scientific leadership and excellence in this research area, to kick-start a competitive European industry in Quantum technologies and to make Europe a dynamic and attractive region for innovate research, business and investment in this field"* [20].

In this thesis we choose the use of superconducting coplanar waveguide (CPW) resonators in the context of quantum optics and quantum information processing. It has been experimentally demonstrated [6] that a single microwave photon stored in a high-quality factor CPW resonator can be coherently coupled to a superconducting quantum two-level system. But before explaining the main advantages of the CPW resonators, a brief review of what is superconductivity, its role in this approach, and some notes on its historical evolution are given.

Actually, in 2011, the Physics community celebrated the $100^{th}$ anniversary of the discovery of superconductivity by H. Kammerling Onnes. Onnes found that the resistance of several metals vanished below a certain material-dependent critical temperature (Tc). A few years later, in 1933, Meissner discovered the second basic property of a superconductor, perfect diamagnetism. He found that a superconductor would expel any magnetic field even if already present when the Tc was crossed. This phenomenon is the Meissner effect. This discovery led to the formulation of a microscopic theory of superconductivity by Bardeen, Cooper and Schrieffer (BSC), in 1957, which showed that a weak attractive force between electrons can led them to form a condensate of bosonic pairs with zero total spin and momentum. This energy state was called Cooper pair and is equal to the gap energy. The BSC theory elucidated the physical origin of superconductivity [14].

Another key element in superconductor quantum electrodynamics circuit (circuit QED) is the Josephson Junction (JJ) [29]. A JJ device is as a superconductor-insulator-superconductor tunnel junction, which can be used as a two-level system [7] or qubit. Our CPW resonator would be coupled to this artificial qubit.

Superconducting properties and CPW resonators offer several advantages for their application in circuit QED [12]. On the other hand, CPWs can be easily designed to operate at specific frequencies, up to 10GHz or higher, and their impedance can be controlled at different lateral size scales. Their small lateral dimensions allow to realize resonators with extremely large vacuum fields due to electromagnetic zero-point fluctuations, a key ingredient for realizing strong coupling between photons and qubits in the QED circuit. Moreover, CPW resonators with large internal quality factors of typically in the several hundred-thousand range can be realized. Their resonant frequency is controlled by selecting the resonator length, i.e. in the few-millimetre order, and its loaded quality factor is controlled by its capacitive coupling with the input and output transmission lines (TL). This planar structure is patterned on a dielectric substrate and can be done by conventional photolithography methods. Superconducting materials commonly used are, for example, aluminium (Al) and niobium (Nb) [4]. Dielectrics typically used as substrates are non-doped silicon (Si) or sapphire ($Al_2O_3$) [13].

In this work we dare to design, fabricate and characterize CPW resonators with well-defined resonant frequency around 7GHz and coupled quality factors about $10^5$. Parallelly, we worked with an experimental group in the Catalan Institute of Nanotechnology (ICN2) where they tested and characterized a circuit QED, based in Josephson Junctions, at very low temperature in their refrigerator. Their experimental results will give the basis to couple our CPW resonator to an artificial qubit.

This thesis manuscript is structured as follows. After this introductory first chapter, the **second chapter** gives an overview of the main theoretical issues concerning resonator properties. This chapter is complemented with Annex I, in which a deeper explanation of Microwave Theory is given. The **third chapter** is dedicated to describe the design development for the CWP resonator, by following the theoretical basis from the first and second chapters and its application. It also includes an overview of the CPW geometry as well as simulations done to predict its behaviour. Some additional results of those simulations are provided in Annex II. Finally, in the **fourth chapter** all the experimental work to fabricate the CPW devices is compiled. As lithographic fabrication procedure laser writer is applied, as a flexible-design patterning technique. Importantly, the laser writer processing is new process, i.e. not established conditions, at the Microelectronics Institute of Barcelona (IMB-CNM-CSIC). As complementary information to this chapter, Annex III describes some methodology issues such as the laser equipment used and the photolithographic procedure followed, Annex IV exposes exemplary tests and results to develop the fabrication process, while in Annex V reports some troubles and difficulties encountered during the different fabrication steps. To conclude, main outcomes are listed and short outlook is given.

## 2. Transmission line theory for microwave engineering

Transmission line (TL) theory [16] brings us the knowledge basis to explain all about the resonator circuit. Its understanding includes the application of field analysis and basic circuit theory before analysing our system, so TL theory is the gap between those two fields. Due to the page limit of the thesis manuscript, the in-depth explanation of the model is introduced in Annex I, which provides theoretical background and allows a better understanding of the origin of the expressions that will appear along this chapter.

### 2.1. General expressions of the transmission line model

In this section the general expressions needed to design our resonating device will be introduced. Detailed in Annex I, we have seen the equivalent circuit for a TL for which we must now analyse intrinsic properties that help defines the TL parameters in a real environment. Figure 2.1 shows relevant parameters for a TL of length l:

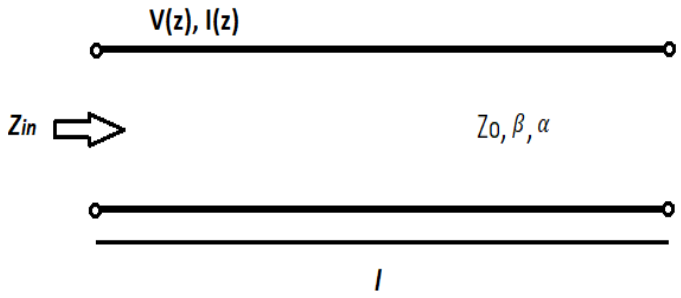


*Figure 2.1. Intrinsic parameters of the transmission line of length l*

Considering a lossless transmission line, with lossless terminations as well, the voltage and current along the line are, respectively,

$$V(z) = V_0\left[e^{-j\beta z} + \Gamma e^{j\beta z}\right] \tag{2.1}$$

$$I(z) = \frac{V_0}{Z_0}[e^{-j\beta z} - \Gamma e^{j\beta z}], \tag{2.2}$$

where Γ is the voltage reflection coefficient and β (rad/m) is the phase constant of the transmission line. β determines the sinusoidal amplitude and phase ratio of the electromagnetic wave that crosses along it. Its expression can be written as,

$$\beta = \frac{w}{v_{ph}} = w\sqrt{LC}, \tag{2.3}$$

i.e. it depends on the angular velocity, w (rad/s), and the phase velocity, $v_{ph}$ (m/s), known as the rate at which the phase of the wave propagates in space.

Another important parameter to describe the properties of a TL is the attenuation constant, α. Its value expresses the total loss of the transmission line. Its natural units are Nepers/m, but we can transform in a more convenient units, like dB/m. There are four types of attenuations [28]:

$$\alpha = \alpha_c + \alpha_D + \alpha_G + \alpha_R, \tag{2.4}$$

where:

- $\alpha_c$ is the loss due to metal conductivity,
- $\alpha_D$ is the loss due to dielectric loss tangent,
- $\alpha_G$ is the loss due to conductivity of the dielectric and
- $\alpha_R$ is loss due to radiation.

In chapter 3, we will explain how the four loss contributions can be neglected if properly choosing materials and geometries for the resonator through different considerations.

With the above parameters we can define a new parameter that describes the signal behaviour of the travelling wave and the circuit components of any TL, the propagation constant, γ. Its expression is,

$$\gamma = \alpha + j\beta. \tag{2.5}$$

where α is the real part and the phase constant (β) is the imaginary part.

Additionally, any media which can support an electromagnetic wave is associated to a characteristic impedance, $Z_0$(Ω). The best way to think about characteristic impedance is to visualise a TL with a normalized length [28], where the $Z_0$ relates with the components of the equivalent circuit as,

$$\frac{V_0^+}{I_0^+} = \frac{V_0^-}{I_0^-} = Z_0 = \sqrt{\frac{R + jwL}{G + jwC}}, \tag{2.6}$$

The impedance can also be seen as the ratio between the positive or negative voltage and current at the peak maximum. Considering a lossless transmission line, i.e. R = G = 0 the $Z_0$, the expression simplifies to,

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{2.7}$$

We will explain the details of why we can neglect the resistance (R) and the shunt conductance (G) in chapter 3. Another important parameter is the input impedance, $Z_{in}$, which describes the impedance of a certain TL length as an arbitrary load impedance, as follows,

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 tan\beta l}{Z_0 + jZ_L tan\beta l}. \tag{2.8}$$

### 2.2. Transmission line resonator

Lumped elements with ideal characteristics are practically unattainable at microwave frequencies, so distributed elements are more commonly used as models. In this section, we will study the TL $Z_{in}$ needed to achieve the type of resonator required for our specific applications. A critical value is the quality factor, Q, of these resonators, which expresses the real study case of lossy TLs.

#### 2.2.1. The open circuit $\frac{\lambda}{2}$ line

To realize a high-quality factor resonator, we will need to design a two sides open circuit structure [16]. Such device behaves as a parallel resonant circuit when the length is λ/2, or multiples of λ/2. The $Z_{in}$ of an open circuit line of length l is

$$Z_{in} = Z_0 \coth(\alpha + j\beta)\, l = Z_0 \frac{1 + jtan\beta l\, tanh\alpha l}{tanh\alpha l + jtan\beta l}, \tag{2.9}$$

Assuming that $l = \lambda/2$ at $w = w_0$, and letting $w = w_0 + \Delta w$, then

$$\beta l = \pi + \frac{\pi \Delta w}{w_0}, \tag{2.10}$$

and so

$$tan\, \beta l = tan\frac{\pi \Delta w}{w_0}\ (2.11)\,, and\ tanh\alpha l = \alpha l \tag{2.12}$$

Combining these results gives a total input impedance as,

$$Z_{in} = \frac{Z_0}{\alpha l + j(\frac{\Delta w \pi}{w_0})}. \tag{2.13}$$

Figure 2.2 illustrates the voltage curves of the two first resonance modes across an open circuit $\lambda/2$ line of length l, where n=1 ($l = \lambda/2$) and n=2 ($l = \lambda/2$).

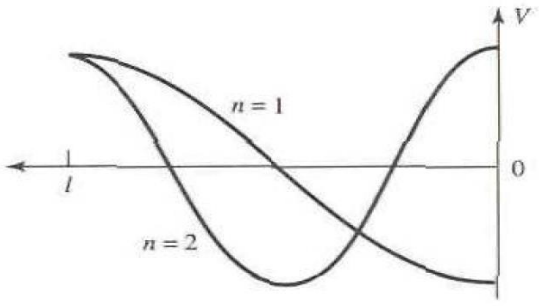


*Figure 2.2 Voltage curves of the two first resonance modes across an open circuit $\lambda/2$ line. Extracted from [16]*

As a reminder, this section is only a reduced version to simplify and condensate the basic considerations of the extended TL theory. For a complete introduction to the above expressions refer to Annex I.

### 2.3. Equivalent circuit model for MW resonators

Since the operation of microwave resonators is very similar to that of the lumped-element oscillators in circuit theory, we will begin by reviewing the basic characteristics of a parallel RLC resonant circuit.

#### 2.3.1. Parallel resonant circuit

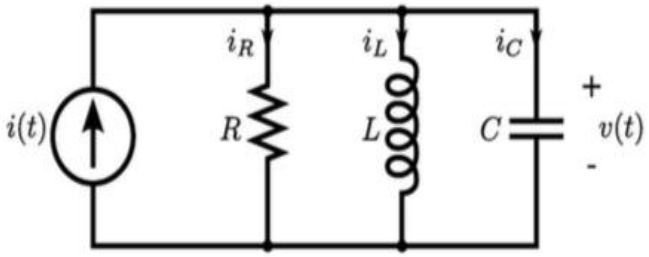


*Figure 2.3. Lumped elements of the parallel RLC circuit. Extracted from [17]*

The diagram of a parallel RLC circuit is shown in Figure 2.3. It consists in, three lumped elements, resistance, inductance and capacitance, connected in parallel, which gives an input impedance [16] as

$$Z_{in} = \left(\frac{1}{R} + \frac{1}{jwL} + jwC\right)^{-1} \tag{2.14}$$

Accordingly, the power that is delivered to the circuit is a complex function as,

$$P_{in} = \frac{1}{2}VI^* = \frac{1}{2}Z_{in}|I|^2 = \frac{1}{2}|V|^2\frac{1}{Z_{in}^*} = \frac{1}{2}|V|^2\left(\frac{1}{R} + \frac{1}{jwL} + jwC\right). \tag{2.15}$$

By definition, the power dissipated by the resistor ($P_{loss}$), the average electric energy stored in the capacitor ($W_e$), and the average magnetic energy stored in the inductor, ($W_m$), are, respectively,

$$P_{loss} = \frac{1}{2}\frac{|V|^2}{R}, \tag{2.16}$$

$$W_e = \frac{1}{4}|V|^2C, \tag{2.17}$$

$$W_m = \frac{1}{4}|I_L|^2L = \frac{1}{4}|V|^2\frac{1}{w^2L}. \tag{2.18}$$

It's known that in the RLC circuit the resonance occurs when $W_m = W_e$. From the average magnetic and electric energy stored expressions, the resonance condition implies a resonant frequency expression as

$$w_0 = \frac{1}{\sqrt{LC}}. \tag{2.19}$$

### 2.3.2. Quality factor of a lumped element resonator

An important parameter of a resonant circuit is its Q, or quality factor, which is defined as the relation between the average energy stored and the dissipated energy per unit time. Consequently, the Q value determines the efficiency of the circuit. Q is expressed as

$$Q = w\frac{(average\ energy\ stored)}{(energy\ loss/second)} = w\frac{W_m + W_e}{P_{loss}}. \tag{2.20}$$

For the parallel circuit in Figure 2.3, the quality factor expression can be rewritten in, the resonance condition $W_m = W_e$, which gives a Q for the resonant circuit as

$$Q = w_0\frac{2W_m}{P_{loss}} = \frac{R}{w_0 L} = w_0 RC, \tag{2.21}$$

This expression shows that for the RLC circuit the Q is directly proportional to R[16].

Near resonance, the $Z_{in}$ can be simplified by using the condition $w = w_0 + \Delta w$, where $\Delta w$ is small, and therefore,

$$Z_{in} \simeq \left(\frac{1}{R} + \frac{1 - \frac{\Delta w}{w_0}}{jw_0 L} + jw_0 C + j\Delta wC\right)^{-1} \simeq \left(\frac{1}{R} + 2j\Delta wC\right)^{-1} \simeq \frac{R}{1 + 2j\Delta wCR} \simeq \frac{R}{1 + \frac{2jQ\Delta w}{w_0}} \tag{2.22}$$

### 2.3.3. External coupling

The Q defined in the preceding section is characteristic of the resonant circuit itself, without any loading effects caused by external circuitry, and so it is called the internal quality factor (Qi=Q). In practice, however, a resonant circuit is invariably coupled to a power source, such as an external circuit. Considering a resonator coupled to a load resistor $R_L$, if the resonator is a parallel RLC circuit, it combines in parallel with the internal resistance R. We can now define the external quality factor ($Q_e$) as,

$$Q_e = \frac{R_L}{w_0 L}. \tag{2.23}$$

Then, the total or loaded quality factor, $Q_L$, can be expressed as the inverse sum of the internal (Qi) and external (Qe) quality factors, i.e. following the expression

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_i}. \tag{2.24}$$

## 3. Designing the CPW resonator

In chapter 3, we will discuss all the dimensions and parameters to be considered for the design, and therefore, fabrication of a high-quality factor harmonic resonator, to be coupled to a superconducting qubit for Q applications. Any electronic device design, starts by understanding its physics, in this case, the analytical expressions explained in Chapter 2 and additional fundamentals in the Annex I. To support its design, we will introduce some simulations of the device architecture, to get a first estimation of how the resonator would work.

### 3.1. Design parameters

There are several aspects to consider in the resonator design. A basic property of the resonator is superconductivity. Considering that it will be operated at very low temperatures; in the order of millikelvin (mK), first, we should decide the material to fabricate the device. The resonator will be fabricated onto a substrate, with its own intrinsic properties, which in turn would have a direct impact on the resonator properties. Finally, an appropriate architecture must be defined for the desired performance.

#### 3.1.1. Material choice

##### 3.1.1.1. Substrate

The substrate chosen for the resonator fabrication is intrinsic, i.e. non-doped silicon (Si). Si wafers are the most widely used substrate in the electronics or microtechnologies sector. Related with its spread usage, the Si properties are well known, while its processing outstands for its versatility and reliability.

Table 3.1 gives us relevant parameters values of silicon at room temperature. $\mathcal{E}_r$ is the relative dielectric constant, $\mathcal{E}_{eff}$ is the effective dielectric constant, $tan\delta_e$ is the loss tangent, which represents the losses when an electromagnetic field is present and $\alpha_d$ is the attenuation due the dielectric losses [16]. A conventional silicon wafer thickness is 500µm.

| Substrate material | Thickness (µm) | $\mathcal{E}_{r(Si)}$ | $\mathcal{E}_{eff}$ | T (K) | $tan\delta_e$ | $\alpha_d$ (Np/m) |
|---|---|---|---|---|---|---|
| Silicon (intrinsic) | 500 | 11.9 | 6.5 | 298 | 0.004 | 0.589 |

*Table 3.1. Important intrinsic (non-doped) silicon properties for the resonator design [1]*

$\mathcal{E}_r$ and $\mathcal{E}_{eff}$ depend on the intrinsic properties of silicon and the surrounding medium. Differently, the $tan\delta_e$ is frequency and temperature dependent. The value in the table for $tan\delta_e$ is for a 10GHz frequency. The effective dielectric constant is the mean value of the relatives dielectric constants of the substrate and the environment. Considering air as the medium, $\mathcal{E}_{r(air)} = 1$, implies that $\mathcal{E}_{eff(Si-air)} = 6.5$.

As introduced in section 2.1, the signal or electromagnetic wave attenuation due dielectric losses is one of the four types of attenuation that contributes to the overall dissipation. For a CPW resonator, the expression for the $\alpha_d$[10] is

$$\alpha_d = \frac{w}{2c_0}\frac{\mathcal{E}_r}{\sqrt{\mathcal{E}_{eff}}} q tan\delta_e \tag{3.1}$$

At low temperatures $\alpha_d$ takes small values that can be neglected as compared to the phase constant, β.

#### 3.1.1.2. CPW structural material. Metal layer

The material chosen to fabricate the resonator is aluminium (Al). This metal is a very commonly used chemical element in microfabrication, e.g. as contact metal or as mask, so its deposition is very well established at the IMB-CNM-CSIC. Its low boiling temperature is perfect to achieve a reliable metallization over silicon wafers. It is a relevant material for its good electrical conductivity and specifically in quantum physics due its superconductivity. Its critical temperature (Tc), the temperature where the metal reaches its superconductor state, is around 1.20K, which is easily reached with available cryogenic technology [14]. In other words, at near-zero absolute temperature aluminium's conductivity tends to infinite ($\sigma \rightarrow \infty$) due the reduction of resistance, associated with conductor losses ($\alpha_c$). Some general aluminium properties are compiled in Table 3.2.

| Metal | Thickness (nm) | Electrical conductivity, σ (S/m) | Tc (K) | Boiling point (ºC) |
|---|---|---|---|---|
| Aluminium | 100 | $3.72 \times 10^7$ (at 298K) | 1.20 | 2480 |

*Table 3.2. Important aluminium (Al) properties for the resonator design. Extracted from [21]*

### 3.1.2. Choosing an architecture

The most common transmission line geometries used in superconducting qubit circuits are the microstrip, stripline and coplanar types. Each of these device architectures has its own advantages and disadvantages, but for our goal, i.e. strongly couple a qubit with the best isolation conditions obtaining a high resonator quality factor, the Coplanar Waveguide (CPW) geometry is chosen.

#### 3.1.2.1. CPW geometry

The CPW geometry proposed by C.P. Wen in 1969 [10] was chosen for this work for additional reasons, precisely, for its easy fabrication as compared to other types of TL structures. Only a single layer is required and fabrication sequence can be reduced to a single patterning step. The CPW structure can be fully fabricated in-house, at the IMB-CNM clean room, and is cheaper and faster than other geometries. Another advantage of the CPW choice is its very small radiation loss, a relevant factor as it would influence the quality factor of the resonator. Furthermore, its characteristic impedance is directly related to the ratio of the width of the inner strip to the width of the gap, so it allows testing the design with various geometries, easily.

Specifying, we have used a conventional CPW shape patterned on a silicon substrate. It consists in a centre strip conductor with large and finite extend ground planes on either side, all made of and aluminium thin film [2]. A scheme of a CPW resonator cross section is shown in Figure 3.1.

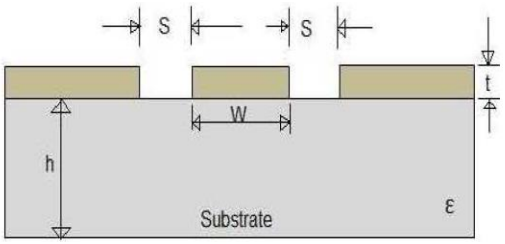


*Figure 3.1. Cross-sectional view of the CPW geometry with the W, S, h and t parameters needed to evaluate its impedance, Zo. Extracted from [31]*

In the Figure 3.1, h is the thickness of the substrate and $\mathcal{E}_r$ is its dielectric constant. The metal thickness of the metal is t, while the width of the conductor and the gaps are given by W and S, respectively. The ratio of W and S determines the characteristic impedance (Zo) of the CPW resonator. The typical Zo of a resonator is 50Ω, so the W/S ratio to achieve this impedance with fixed h, t and $\mathcal{E}_r$ is defined in Table 3.3.

| h (µm) | t (nm) | $\mathcal{E}_r$ | W (µm) | S (µm) |
|---|---|---|---|---|
| 500 | 100 | 11.9 | 10 | 6 |

*Table 3.3. Numerical values of the CPW geometry for the resonator design to achieve a Zo of 50Ω [9].*

In terms of wave propagation [8], when an electromagnetic wave travels along a TL of CPW geometry it flows parallel to the ground introducing a driving field in both sides of the central conductor. Due to the symmetry, the grounding at both sides, the energy of the photons can be isolated from the environment, the energy levels are confined and then the qubit could be strongly coupled with the electromagnetic waves. Figure 3.2 shows a simplified scheme of this concept.

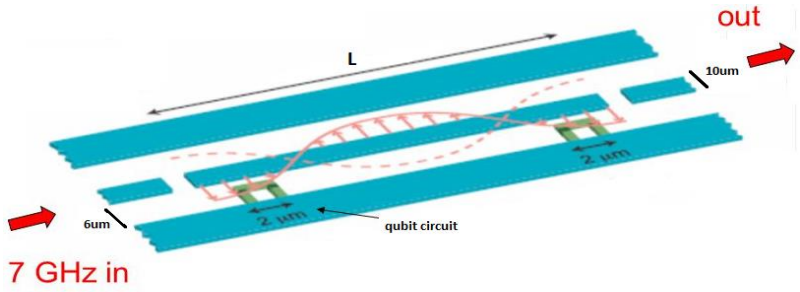


*Figure 3.2. EM waves travelling along a CPW resonator coupled to a superconducting cubit. Extracted from [18]*

Based on this small radiation loss we can perform a resonator with a high-quality factor and neglect the attenuation due to radiation ($\alpha_R$) [5] referred in section 3.1.2.

#### 3.1.2.2. Parameters

Since the TL model is general, the device can be designed as the parameters R, L, G and C per unit length are determined. With the Al-Si stack, the conductance G is negligible, as the attenuation due the loss in the conductivity of the dielectric ($\alpha_G$) because of the small separation between the conductors is low and, therefore, can be removed from the TL circuit model. Thus, the CPW geometric contribution to inductance and capacitance per unit length [9] is

$$L_l = \frac{\mu_0}{4}\frac{K(k_0')}{K(k_0)}, \tag{3.2}$$

$$C_l = 4\mathcal{E}_0\mathcal{E}_{eff}\frac{K(k_0')}{K(k_0)}. \tag{3.3}$$

In these equations, K is the complete elliptic integral of the first kind with geometric arguments as

$$k_0 = \frac{w}{w+2s}\ (3.4), and\ k_0' = \sqrt{1-k_0^2}. \tag{3.5}$$

From the reported literature [13] and online simulators assessment [19] we can extract our values for the inductance and capacitance per unit length, which depend on the CPW geometrical relations: the conductor width, the gap width and the length of the transmission line, which we will discuss later, are the main ones. For our resonator design, we get

| $L_l$ (H/m) | $C_l$ (F/m) |
|---|---|
| 4.23x10-7 | 1.71x10-10 |

*Table 3.4. Numerical values for the inductance and capacitance per unit length of the resonator*

Using these values in Table 3.4. we are able to compute the phase velocity of the TL theory from,

$$v_{ph} = \frac{1}{\sqrt{L_l C_l}} = \frac{c}{\sqrt{\mathcal{E}_{eff}}}. \tag{3.6}$$

Note that, compared to expression 2.3 in chapter 2.1 for the phase velocity, we have introduced the capacitance and inductance per unit length. The reason is the normalized length of the resonator that we are considering here, as well as, some geometry parameters.

The last step before analysing the equivalent circuit of the resonator is to define the total length needed to achieve a given resonant frequency ($w_o$), in our case, in the range of the GHz. As the refrigerator available in ICN2 can only reach frequencies between 4-10GHz, we decided to design a resonator with a $f_0 = 7GHz$. If we know (from section 2.2.1) that we have approximated the resonator as an open circuit λ/2 line, the total length can be calculated from expression (see equation AI.16 from Annex I) [9]

$$l = \frac{\lambda}{2} = \frac{v_{ph}}{2f} = \frac{c}{2\sqrt{\mathcal{E}_{eff}}}\frac{1}{f}. \tag{3.7}$$

For a frequency of 7GHz, the total length will be *l*=8.404mm.

Finally, we can now calculate the last CPW intrinsic parameter, its phase constant,

$$\beta = \frac{2\pi f}{v_{ph}}, \tag{3.8}$$

where the total attenuation can be neglected, i.e. α=0.

| $v_{ph}$ (m/s) | α (Np/m) | β (rad/m) | $l\ (mm)$ |
|---|---|---|---|
| $1.18x10^8$ | 0 | 373.78 | 8.404 |

*Table 3.5. Transmission line intrinsic numerical parameters after compute the total resonator length*

### 3.1.3. Equivalent resonator circuit

In order to operate the resonator circuit, we must somehow couple externally our measurement input and output signal to the device. In the case of the device we are examining, this coupling can be modelled as a pair of input/output capacitors connected to ground by load resistors as shown in Figure 3.3.

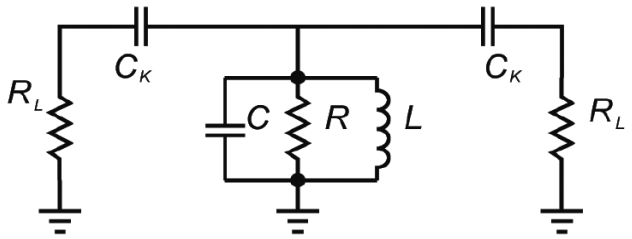


*Figure 3.3. Parallel RLC circuit (center) with capacitively coupling (sides). Extracted from [13]*

Though only a single resistor and a single capacitor have been added to each side of the CPW device, there is no longer a trivial way to extract the total quality factor, Q of the loaded system. Yet, we can simplify the problem by performing a Norton equivalency [13] of the coupling, the series resistor $R_L$ and capacitor $C_k$ can be viewed equivalently as parallel capacitor $C^*$and $R^*$, as depicted in Figure 3.4.

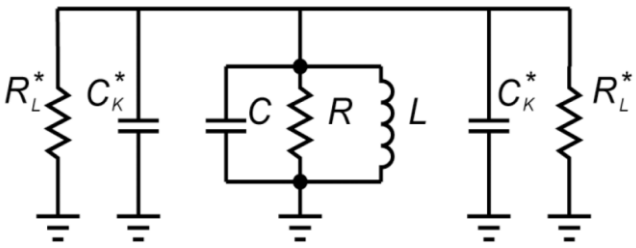


*Figure 3.4. Norton equivalent of the resonant coupled circuit. Extracted from [13]*

Accordingly, the expressions for Norton equivalences, which are frequency dependent, are

$$R^* = \frac{1 + w_n^2 C_k^2 R_L^2}{w_n^2 C_k^2 R_L}, \tag{3.9}$$

$$C^* = \frac{C_k}{1 + w_n^2 C_k^2 R_L^2}, \tag{3.10}$$

$w_n = nw_0$ is the angular frequency of the integer number mode of the resonance.

In our design, we specifically want an asymmetric capacitively coupling, so that we can achieve directionality in the power that flow along the transmission line. In other words, an asymmetric coupling assures that the whole source power flows toward the output. Therefore, we will have two different values for each one of the above equations (3.9 and 3.10) from the equivalent $R^*$and $C^*$, determined by the capacitance of the capacitors coupled to the resonant circuit.

To achieve this directionality in the delivered power, we chose specific values for the two external quality factors, one for the input coupling (left-side in Figure 3.4) and other for the output's (right-side in Figure 3.4). Those quality factors values are $Q_{ext1} = 10^5$ and $Q_{ext2} = 10^4$, respectively. The higher quality factor the more the power flow and less retention. From the circuit and expression 2.23 seen in and section 2.3.3 we can obtain an expression for the external quality factor as

$$Q_{ext} = \frac{w_n R^* C}{2} = \frac{C}{2 w_n R_L C_k^2} \tag{3.11}$$

Putting some numbers, a loaded resistor $R_L = 50\Omega$ for matched circuits (see Annex I) and knowing that the angular velocity is $w_n = n2\pi f$, where n=1 and f=7GHz, the following values are obtained (Table 3.6).

| $\boldsymbol{Q_{ext,n}}$ | $\boldsymbol{C_k\ (fF)}$ | $\boldsymbol{R^*}$ **(Ω)** | $\boldsymbol{C^*}$**(fF)** |
|---|---|---|---|
| $Q_{ext1} = 10^5$ | 1.28 | 6305335.74 | 1.27 |
| $Q_{ext2=}\ 10^4$ | 4.04 | 632989.08 | 4.04 |

*Table 3.6. External quality factors of the asymmetric capacitively coupling and their capacitances*

Now, by assuming the parallel capacitors and parallel resistors, the complete circuit system can be reformulated as a single RLC parallel resonator whose quality factor represents that of the whole loaded system, $Q_L$

$$Q_L = w_n^* \frac{C + C_1^* + C_2^*}{1/R + 1/R_1^* + 1/R_2^*}. \tag{3.12}$$

In addition to estimating $Q_L$, this model indicates that increasing the coupling capacitance decreases the resonance frequency as,

$$w_n^* = \frac{1}{\sqrt{L_n (C + C_1^* + C_2^*)}} \tag{3.13}$$

Finally, to find the intrinsic values L, R and C of the internal resonant circuit [9] we must compare the expressions of the input impedance $Z_{in}$ from the lumped element circuit model (section 2.3.2, eq.2.22) and the transmission line theory (section 2.2.1, eq.2.13). Using this approximation, then, we obtain

$$R = \frac{Z_0}{\alpha l}, (3.14),\ \ L = \frac{2 L_l l}{n^2 \pi^2}\ \ (3.15)\ \ and \quad C = \frac{C_l l}{2}, \tag{3.16}$$

which numerical correspondence is summarized in Table 3.7.

| **R (Ω)** | **L (nH)** | **C (pF)** |
|---|---|---|
| 0 | 72.2 | 73.1 |

*Table 3.7. Lumped-element values of the internal harmonic resonant circuit after comparing TL and circuit models.*

#### 3.1.3.1. Quality factor

Considering its asymmetric coupling, the expression for the loaded quality factor, $Q_L$ (see section 2.3.3 and equation 2.24), becomes

$$\frac{1}{Q_L} = \frac{1}{Q_i} + \frac{1}{Q_{ext1}} + \frac{1}{Q_{ext2}}, \tag{3.17}$$

where the two external quality factors appear now in the final expression. But our working resonator would be operated at the so-called over-coupled regime [9]. This means that $Q_i > Q_{ext}$, so that the total or loaded quality factor becomes

$$\frac{1}{Q_L} \simeq \frac{1}{Q_{ext1}} + \frac{1}{Q_{ext2}} \tag{3.18}$$

This approximation can be applied in relation to the effect of the superconductivity of the metal, at very low temperatures (mK), all the losses inside the circuit are neglected and the conductivity becomes infinite, so neglectable are also the dielectric losses [11]. Therefore, the internal quality factor, which depends only on the lumped-element circuit and excludes the external coupling, must be very high, much larger than the external. To sum up, the CPW resonator explained in this chapter is designed to have a loaded quality factor of $Q_L = 18636.45 \simeq 10^5$.

### 3.2. CPW simulation by Sonnet Software

The software used to simulate the high-quality resonator system is Sonnet software. As their literally comment in their web-side, [30]: *"Sonnet is best suited to design challenges involving 3D planar circuits, which consists of layers of metal traces embedded in stratified dielectric material. Sonnet allows any number of dielectric/metal layers including multiple user defined metal types and dielectric materials."* Some examples of 3D planar circuits include CPW, which is our main purpose.

#### 3.2.1. The transmission spectrum

The TL spectrum, also referred as $S_{21}$ of a half-wave resonator in a 2-port configuration can be measured using a Vector Network Analyser (VNA) and is typically a Lorentzian peak at the resonance frequency, $f_0$ [16]. The Sonnet software is based on a multiport network that can be measured through its scattering parameters. Definition of the scattering matrix parameters is detailed in Annex II. The sharpness of the peak is used to quantify the quality factor of the resonator, i.e. it can be calculated by the ratio of the magnitude of transmission ($Q_L$=$f_0$/ $\delta f$), between the resonance frequency and the full-width half-maximum ($\delta f$), which is located always at 3dB above the maximum [9]. The Lorentzian-shaped transmission spectrum is given by the expression

$$P_{(f)} = A_0 \frac{\delta f}{(f - f_0)^2 + \delta f^2/4}. \tag{3.19}$$

### 3.2.2. Resonator design

Firstly, for the Sonnet simulation we must define which materials constitute the different layers, as well as their thickness and the contour conditions. The theoretical expressions by which we have modelled the ideal resonator design consider air as the medium where the resonator is operated, so we should add two air layers (1000µm thick) on both the top and the bottom of the Si-Al stack. Additionally, free-space contour conditions were fixed in order to fit with the Maxwell Equations used in the electromagnetic analysis of the lumped element circuit. The available circuit QED chips at ICN2, which fits in the refrigerator stage, are 7x3mm$^2$ size. Therefore, the 2D resonator conformation is purposely adjusted to fit this size. Figure 3.5 shows a depiction of the box used in the simulation.

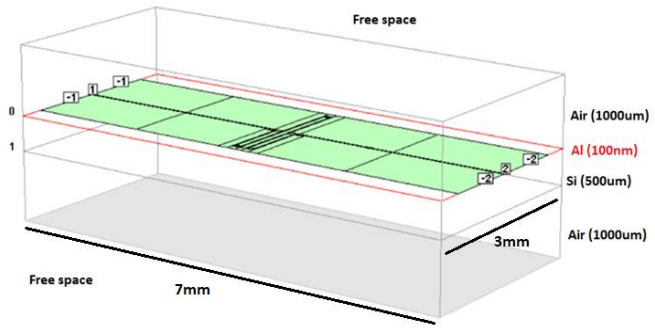


*Figure 3.5. Sonnet simulation 3D box by which all the layers of the theoretical model are*

Secondly, the total resonator length needed, to operate at 7GHz, is found to be 8.404mm. This length is larger in absolute value than the chip size, so a meander geometry has been chosen to compact the size of the resonator while maintaining the resonance characteristics. Following electromagnetic wave theory, the meanders are separated 100µm to avoid interferences from the radiation of its neighbour transmission line. Relatedly, with this geometry we would avoid losses due to the radiation attenuation, i.e. achieving a high-quality factor performance. Moreover, according to CPW geometry conditions, a centre transmission line of 10µm width was designed and separated by a 6µm gap from the ground planes, so that a characteristic impedance of 50Ω is obtained. Ports must be defined at the edges of the box: port 1 and 2 represent the flow direction of the delivered power, read as the $S_{21}$ spectrum; ports -1 and -2 fix the same constant voltage at the ground planes. In addition, the capacitors have been also simulated to provide the suitable capacitances, and therefore, included into design, for which further description is given in Annex II. Figure 3.6 schematizes the described design.

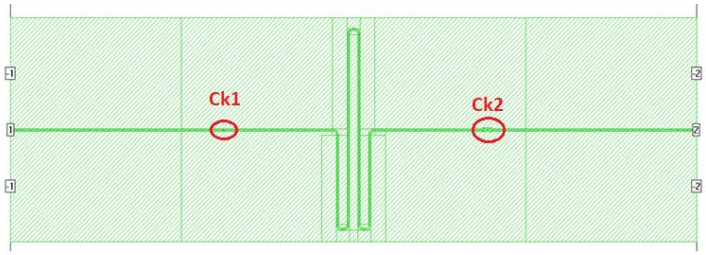


*Figure 3.6. 2D view of the planar resonator design used for the simulation (without the external connectors) and capacitors as "insets".*

From the Sonnet design, we simplified some aspects due computing simulation time. Specifically, we missed the connectors for input and output signals that should connect the 10µm width line with the refrigerator external circuit. Practically, provided the actual connector size (typically, 300x300µm$^2$), connectors must be related to the transmission line size, in particular, with a slope which maintains the characteristic 50Ω impedance. Even though connectors are not present in the Figure 3.6, the appropriate slope had been simulated and optimized aside and introduced in the fabrication design.

### 3.2.3. Simulation results

Finally, when the design is finished the final step is running simulation. Upon results from the given response, we can analyse the Lorentzian shape to extrapolate the loaded quality factor, $Q_L$. By sweeping the response in a frequency range between 1-20GHz we obtain the plot depicted in Figure 3.7, in which the transmission line spectrum $S_{12}$ (dB) versus frequency (GHz) is represented.

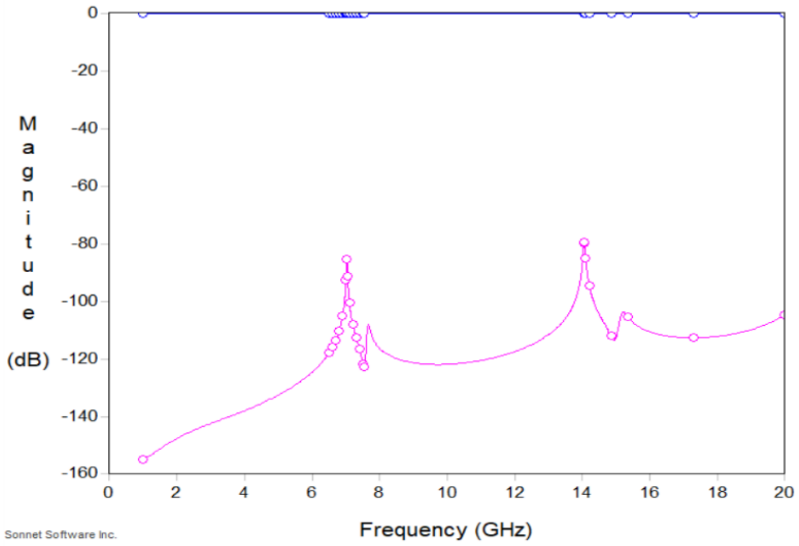


*Figure 3.7. Transmission line spectrum $S_{21}$ of the first approximation of the two first modes of the resonant frequency (7GHz and 14GHz) by simulating the resonator with symmetric coupling by two parallel capacitors 50µm gap. Power (dB) vs frequency (GHz).*

For this first swept, the analysis of the graphic in Figure 3.7 has been done by considering a symmetric capacitive coupling considering parallel capacitors separated by a 50µm gap, which give a rough capacitance of 0.12fF (see Annex II). Before starting to search for errors in the designed resonator, we wanted to make sure that the length of the transmission line fitted with the associated frequency. The lower the capacitance of the capacitors coupled to the internal circuit, the larger the quality factor (see equation 3.12). From the graphic, we can correlate the Lorentzian peaks as the position (frequency) where the resonance occurs. We find the resonances at 7GHz and 14Hz, corresponding to the first and second mode, respectively. However, the quality factors of the Lorentzian peaks are very poor, and do not agree with the aimed ones. Similarly, we still have the same problem when we simulate the final design from Figure 3.6: in a range between 5.5-7.5GHz we get the shape in Figure 3.8. The quality factor obtained from

the peak is $Q_L(simulated) = 49.92$ while the designed $Q_L(designed) = 18636.45$, so we obtain a quality factor 373.32 times lower $\left(\frac{Q_L(designed)}{Q_L(simulated)} = \frac{18636.45}{49.92} = 373.32\right)$ than the expected.

After getting these disappointing results, we have changed some conditions in the software design with the idea of finding a solution for the problem, but the efforts were useless. The problem is supposed to be only with the reliability of the quality factors, because the resonant frequency shift due to the addition of the external circuit is present (remember equation 3.13 from section 3.1.3), where we have effectively seen that by *"increasing the coupling capacitance decreases the resonance frequency"*. Numerically, we get $w_1^* = 4.14x10^{10} rad/s$, or $f_1^* = 6.5x10^9 GHz$, which is in good agreement with the obtained result as shown in Figure 3.8. The numerical calculations have been checked and validate for other more experienced group members and compared with some existing literature [9], so we assume the problem is about parameters used by the Sonnet Software.

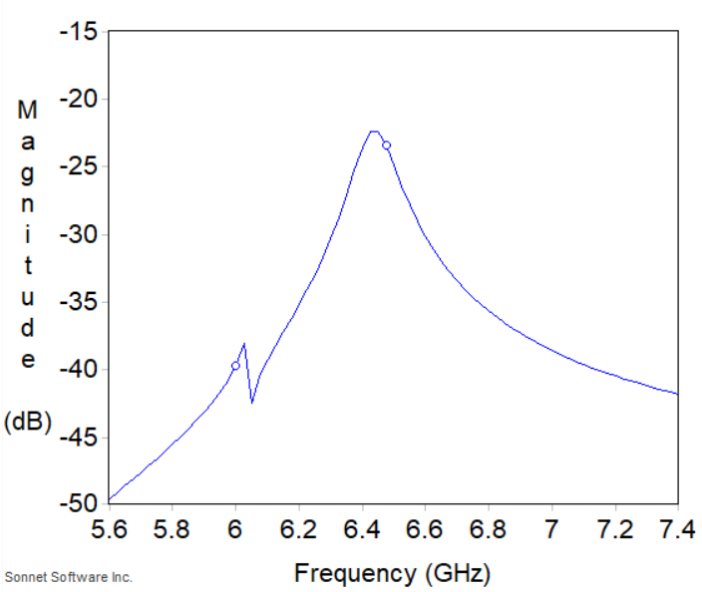


*Figure 3.8. Transmission line spectrum $S_{21}$ by simulating the final resonator with asymmetric coupling by two interdigitated (3+2 and 1+1) capacitors. Power (dB) vs frequency (GHz).*

Therefore, and to not fully block the project progress with this difficulty, a disagreement in the quality factor value, both experimental groups agreed to maintaining the original fabrication design and only redefining the way and target we would focus for the fabrication development. Accordingly, instead of pursuing at the high-quality factor for the operational resonator we would concentrate in proving experimentally if the design fits with the resonance frequency we have modelled. In other words, the fabrication will be executed to find out if the resonator operates at the GHz frequency regime, and specifically at ≃7GHz. The capacitance of the capacitors, the total transmission line length, the meander shape, the connectors size and all the other parameters will be the same as planned in the design.

## 4. Resonator fabrication

In this chapter we will explain the basic steps of an aluminium resonator fabrication and some results of its actual technology development during this project. We will start by presenting the fabrication strategy chosen, followed by a deep explanation of the patterning technique, its design and exposure strategy, adapted and constraint by the equipment used, for finally presenting and discussing some of the experimental results.

### 4.1 Precedents and fabrication strategy

As it has been mentioned previously, it is the first time that a group of experimentalist and technologist endeavours, regionally and nationally, to realize a project involving fabrication of domestic chips for quantum applications. The involved researches, P. Forn-Díaz and G. Rius, accumulate enough background knowledge and experience in characterization and micro/nanofabrication related to the matter of interest, yet a collaborative work using the regionally-available fabrication capabilities, for instance of the IMB-CNM-CSIC, have not yet been used, even if process flow in fabrication technology has not significantly changed. Practically no previous documentation or experience in fabricating, e.g. superconducting circuit qubits, are therefore owned. Additionally, the chosen patterning technique, direct writing lithography, had been recently installed at the SBCNM at the moment to start this project, so no previous experience, for instance, regarding exposure strategy or conditions, was available.

By regarding the dimensions of the resonator as designed in chapter 3, it can be seen that the geometry involves large size order, from the millimetre of the whole circuit structure, elements of hundreds of microns to units of microns, i.e. the connectors dimensions are 300$\mu m^2$, which connect with the transmission line of 10µm width and terminate with interdigitated capacitors of 2µm finger width and gap separation. Actually, the shape of the device is complex, e.g. the meanders are not a trivial geometry to be made with elementary design and lithography techniques, as well as the symmetry of the finger capacitors, which were challenging due to the nominal resolution of the available laser head (~1µm, in very best conditions).

Some literature [15], [2] has established that the best fabrication process which gives the appropriate results in terms of resolution and superconducting qubits reliable and performance involves an etching process, which pathway is schematized in Figure 4.1. (left-side).

Etching step in micro/nanofabrication can be either a chemical (wet) or a physical (dry) process (or a combined phenomenon) to, for instance, selectively remove unprotected parts of a metal surface or a silicon film by means of patterned photoresist mask. For our specific case, single digit micrometre resolution for etching a 100nm thick aluminium film while preserving the atomic smoothness of the Si substrate, a recipe and equipment for dry etching. For us as well, as the laser lithography was already a whole process step to be started from scratch, an alternative more affordable fabrication strategy was chosen, in order to be able to produce a first prototype of the resonator during the period of this project. The chosen pattern transfer sequence is, instead, using laser lithography and then thermal evaporation of the thin metal film, plus lift-off of the photoresist, which procedure is shown in Figure 4.1 (left-side).

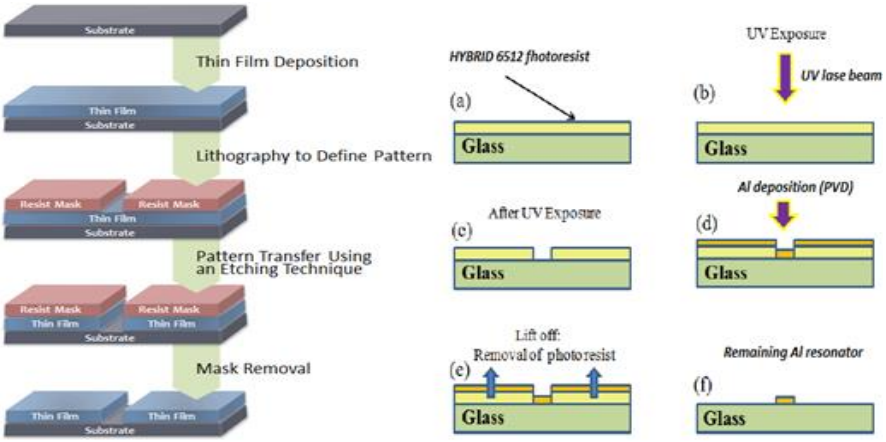


*Figure 4.1. Left-side. Etching process pathway needed to transfer a pattern onto a substrate, starting with a thin film deposition, the pattern transfer using etching and the mask removal. Extracted from [24]. Right-side. Lift-off process pathway needed to transfer a pattern onto a substrate, starting with a coating of the photoresist, the pattern transfer by UV laser beam and the thin aluminum film deposition. Extracted from [25]*

As the design and fabrication is in prototyping early stage, i) flexible-design patterning technique (laser writer) was chosen and, as for pattern transfer, ii) metal deposition plus lift-off of the resist, is applied (Figure 4.1 right-side).

Finally, another aspect to be considered is the state of art of the equipment used for the resonator fabrication. Instead of the traditional photolithographic procedure, by which the photoresist is exposed though a mask with high-intensity ultraviolet light, a direct UV laser writer technique has been implemented. The equipment is called *KLOE Dilase650,* which came to the IMB-CNM-CSIC in September 2018, only one month before this project started. No one in the centre had ever worked with this technology before, either SBCNM engineers or IMB researchers. It was completely new for everyone. Therefore, we have work gradually to optimize all the equipment parameters during the realization of this work.

In the following sections, all the aspects related with the experimental work and fabrication development to be established or optimized and combined will be deeply explained, including particular adjustments which have been implemented in the fabrication sequence and steps, so that a first prototype of the resonator that, in addition, has to eventually agree with the results of the simulations introduced in section 3.2.3, is obtained. Due the size constraints of this manuscript, some previously established photolithographic procedures and conditions which had to be have been included as an appendix, Annex III, even if completely new for this author. These include: the cleaning and spin coating of the wafer with a certain positive photoresist and subsequent technique for metal thin film deposition.

### 4.2. General equipment description

The Dilase 650 by Kloè [27] is a direct writing laser photolithography equipment. It is designed to materialize micrometre patterns in photoresists films by a photopolymerization process, which is induced by a UV laser beam exposure. Specifically, its basic technical principles and writing capabilities include:

- Contouring writing on both XY trajectories axe.
- Dynamic and continuous writing.
- Writing suitable mostly on planar substrates.
- Writing for both negative or positive resins, those photosensitive at the laser wavelengths.
- Exposure time optimization by choosing nominal laser spot size of 1µm or 10µm.

The software is divided into two separate elements that control different aspects of the design and exposure implementation. Respectively, the so-called "*Kloédesign*", allows us to import the design in e.g. a GDS format and define the laser trajectories on it, generating an LWO file type; and "*Dilasesoft650*", which can only import the LWO files previously generated, in which we can define the actual lithographic laser conditions for writing. So, the general design and conversion path we have followed for the exposure of the resonator designed in chapter 3 is as follows:

1. Design of the resonator with GLADE software and export the file in GDS format.
2. Import the GDS file into "*Kloédesign"* software, where we can: define, optimize and simulate the laser trajectories for each of the parts of the resonator. Then, it is exported in LWO file format.
3. Import the LWO file into the "*Dilasesoft650*" software and define all the exposure and dose conditions of the laser writer (scan speed, laser head, etc.).

As mentioned, full description of the equipment, laser writing protocol and more details of above pathway are given in Annex III. We strongly recommend the reader to read this part before continuing if not familiar with the technique.

As it has also been said, the laser writer was not a consolidated process in the IMB-CNM-CSIC, so the machine was new for all. Due to this fact, actually this work was the first application that was attempted, and therefore, we had to experience and to optimize every single step, which, in fact, has importantly contributed for all to get familiar with it. Particularities include: the importance of files conversion, choice of the laser trajectories and definition of the multiparameter exposure conditions. Yet, we did not have started completely from zero, technicians from the centre had done preliminary tests and acknowledged. Their previous tests had consisted in exposing arrays of isolated lines over a silicon wafer covered with a thin silicon oxide (SiO2) layer. They had found some initial dose and speed conditions to control line widths, which were determined by scanning electron microscopy. We based our initial exposures on those tests, but despite their accuracy, we have had to design the complex structure resonator, patterning was done, instead, onto silicon wafers, so many experiments and adaptations have been necessary

### 4.3 GLADE resonator design

The first step is to create a GDS file with the resonator design which enabled to be read with the "*Kloédesign*" software. This kind of file is generated thanks to graphical user interface builder called GLADE software [23], which is often used to fabricate photolithographic masks for optical lithography. As we have explained in section 3.2.3, the simulation did not give a high-quality factor from the $S_{21}$ spectrum. Thus, we decided to check only if the designed resonator is consistent with calculated resonant frequency. A CPW resonator structure (Figure 4.2 top) is no longer needed to achieve this goal, because its resonant frequency not depends on the CPW geometry (i.e. resonator surrounded by grounding plates). The

resonator will still maintain a characteristic impedance of 50Ω and the same intrinsic parameters. Therefore, we changed the original CPW design to its complementary shape, which is coherent and convenient for the chosen fabrication process. Figure 4.2 shows the original resonator geometry if the etching process which would have been used in the fabrication (Figure 4.2 top) and the new geometry used to make the prototype by metal deposition plus lift-off processing (Figure 4.2 bottom).

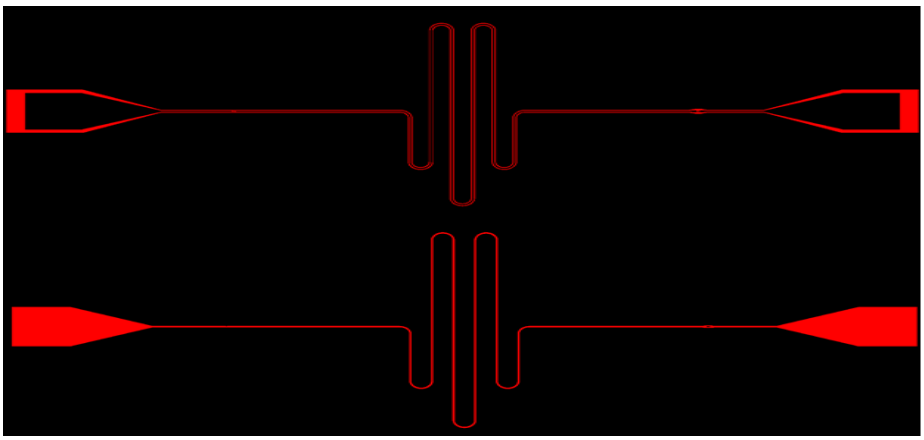

*Figure 4.2. Original (top) and new (bottom) resonator design made by GLADE which will be exported as GDS file. There is no scale length available in the software, but the total size of the image (for each resonator) is 5x2mm².*

For clarity, polygons coloured in red would be the parts to be exposed by the UV laser beam. In Figure 4.2 (top), red areas would be the gaps between the transmission line and the ground planes. But due to the chosen fabrication procedure, in the complementary design showed in Figure 4.2 (bottom) the ground planes have been deleted and the red polygons represent the transmission line, i.e. the resonator. The result after the lift-off process will, therefore, be an aluminium resonator without ground planes, which could not have applications in the quantum information by qubits, but its resonant frequency would have been determined by design. In this sense, the final device will be equivalently operative.

### 4.4. Exposure strategy and parameters of lithography

Now we must define each of the laser trajectories in order to obtain the pattern, first, on the photoresist, and, then, transferred onto the silicon wafer. First, we should import the GDS file in the *"KloéDesign*" software, in which the design from Figure 4.2 (bottom) is shown. The software allows correcting errors due file conversion, as well as simulating all the laser trajectories that will have to be used to create the pattern by exposure. It is important to know how the laser beam delivery will be driven during the exposure, so a study of the simulation has been necessary. For instance, it is the motion of the equipment stage what controls the pattern exposure. The laser beam head is always fixed, in the same position. Relatedly, the stage can precisely move in the XY direction, but not curved trajectories can be done. So, for the curved elements that constitute our meander design and the connectors slopes, the best laser writing trajectories and mode must be tested. Differently, the resonator has basically horizontal or vertical shapes which are more easily optimized because as they fit with the XY motion of the equipment stage.

Moreover, there are some basic parameters of the lithography that determine e.g. the resolution of the exposure zones. With the previous tests of IMB-CNM-CSIC technicians we had for instance, an idea of the

dose we should apply to obtain ≃1µm width isolated lines. Starting with this information, we began our tests, but as our design was more complex than simple lines, a number of exposures were needed to calibrate and obtain good accuracy. The basic exposure parameters to be defined and optimize have been:

- The focusing height: the distance between the focus head and the wafer surface, in mm.
- The writing velocity: the moving velocity of the XY motion stage during exposure, in units of mm/s.
- The return velocity: the speed of the motorized stage during the repositioning between two separate functional lithographic trajectories, in mm/s.
- The delivered beam power: the fraction of laser power available at the output of the focusing lens to expose the photoresist during the writing. It is called modulation and is computed by the % of power delivered to the target.

The focusing height, which is deeply explained in ANNEX III, depends on the thickness and type of photoresist, the substrate and is related with the Z resolution of the pattern. A focusing height always around -2.165mm was found for the 1.4µm thick HYBRID photoresist on 500µm thick Si wafer. The photoresist thickness is not always so precisely-fixed, at 1.4µm, e.g. it can slightly change due some variations due to its deposition or issues with the placement of the chip on the laser stage. Yet, focus variations were minimal, and in average a fixed value of -2.165±0.1mm focusing height was used. The writing velocity seemed not as critical as the focusing height, as long as the speed was not too fast. For instance, we used 0.5mm/s for all exposure tests.

The shape of the laser beam intensity is typically understood as a Gaussian distribution. The lateral resolution or separation between raster line scans for area elements will then depend on how sharp the Gaussian profile is and how close are them. The minimum resolution could be in principle attained with the smaller laser head, and we assume that a resolution around 1µm is feasible, if the equipment and exposure conditions are well optimized attributed to the full width at half maximum (FWHM) of the beam profile.

Furthermore, the writing velocity of the laser exposure changes the control and parameters of the beam delivery. Logically, the smaller the stage velocity the less distance is travelled in a fixed time. We have effectively seen that this is critical in closely separated, but large, elements, such as the condensers. Moreover, the modulation refers to the peak intensity, but not its sharpness. For determining separation of two parallel laser trajectories separated a distance x, the Gaussian shape light intensity delivered to the photoresist would be like showed in Figure 4.3. Depending on whether we want to obtain isolated lines or an area, modulation, stage velocity and separation have to be defined experimentally.

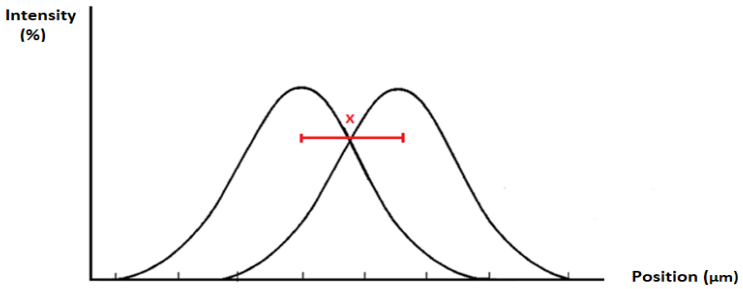


*Figure 4.3. Shape of two parallel laser beams: Gaussian distribution.*

Appropriate modulation and stage velocity in combination with trajectories separation will have to be found for obtaining the pattern width and resolution desired. Otherwise, we can get over or underexposed/developed zones, for instance, in areas, and not well-defined edges that would change the sizes of the original design (Annex IV and V show some examples). This is why, the scan trajectories strategy is as important and longly explained as follows.

After several tests, we have been able to establish an optimized exposure strategy for dealing with the large, small, complex shape and demanding-resolution elements that our resonator is composed of. The strategy involves dividing the whole resonator exposure in 5 polygons, of which two isolated structures, correspond to the interdigitated capacitors. Not only this, they had to be individually exported in LWO format in the software, so that we can make them attribute two different laser trajectory modes:

- Filling mode: all the polygons are filled up by a finite number of parallel laser trajectories. Every single trajectory has a width determined by the dose applied, which must to be defined by either modulation or velocity. This combination will change the Gaussian distribution shape explained above, giving its respective exposure resolution. We have chosen a separation (spot size) of 1µm because it was the only verified data we had. Those 5 polygons partitions, with their laser trajectories simulations, are showed in Figure 4.4.

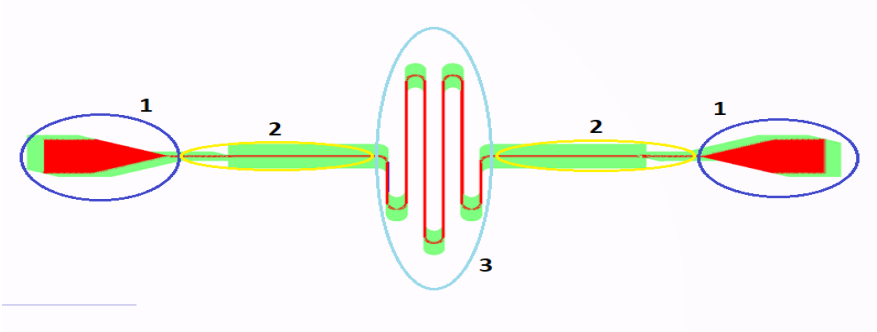


*Figure 4.4. Resonator partitions and laser trajectories simulation made by the Kloé Design software and exported as LWO file*

As it can be seen in Figure 4.4, we have split the five elements in (only) three different groups, as there is certain symmetry. Each group has been filled with the mode that best fit with its geometry in order to optimize writing times and resolution. Examples of different filling modes can be seen in Figures 4.5, as they gave us the best results. Reasons of their choice are:

1) *Optimized filling mode* has been chosen for the connectors because of their slope. It also showed that it can correctly connects with the 10µm width transmission line.

2) *Horizontal filling mode* is used to fill the horizontal transmission line, because its linear geometry is completely coincident.

3) *Vertical filling mode* better agrees with the long vertical part of the transmission line in the meander shape part.

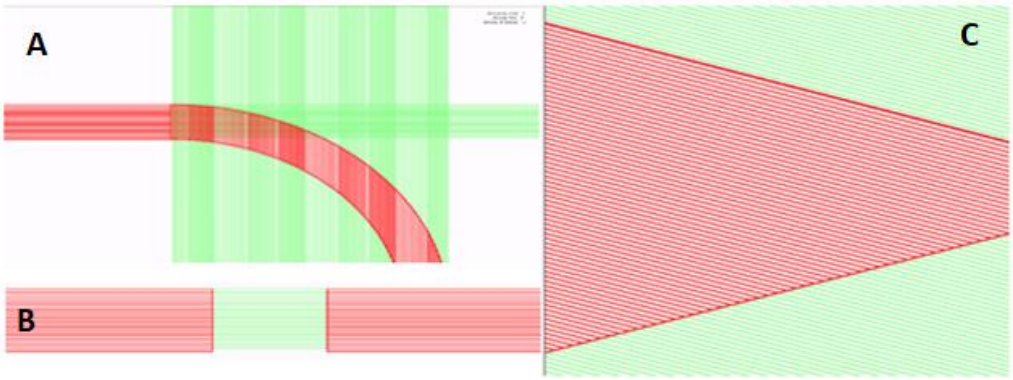


*Figure 4.5. A) Vertical filling mode laser trajectories. B) Horizontal filling mode laser trajectories, typical gap (or fingers in interdigitated structures) separation is 2µm. C) Optimized filling mode laser trajectories. Where the red lines are the laser trajectories mode ON and the green lines laser trajectories mode OFF.*

- Contour mode: the resolution required for capacitors in the limit of the laser writer capabilities were addressed with this mode. The close dimensions of the capacitors to the minimum resolution of the laser beam made them the more critical part of the whole design. Each line in Figures 4.6 and 4.7 is one laser (stage) trajectory, but it will be exposed once. Besides, the exposure dose has been chosen to get a line width of 1µm, according to conditions found in complementary tests. Instead of an area element, the condenser is defined as four horizontal lines, to achieve the 4µm width in the case of the interdigitated 1+1 capacitor and two to fit with the 2µm of the 3+2 interdigitated. In addition, two vertical parallel lines have been used, so 2µm width in total, at the edges of the capacitor to ensure a good lateral resolution, match, between the areas exposed using filling versus contour modes. Tests that had shown serious irregularities at the boundaries caused by the overlap/overexposure (see Annex IV) when using the two modes linking elements could be obtained with this corrected design.

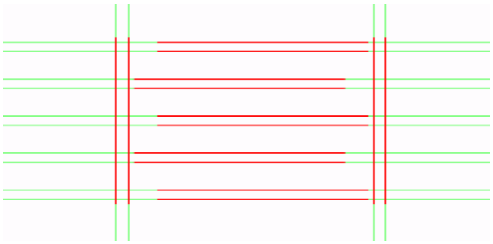

*Figure 4.6. Interdigitated 3+2 capacitor with contour mode laser trajectories*

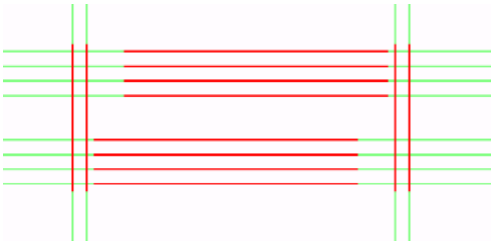

*Figure 4.7. Interdigitated 1+1 capacitor with contour mode laser trajectories*

Once we have defined optimized lithographic laser trajectories the LWO files needed to import with the *"Dilasesoft650"* software can be generated. We exported three different LWO files, containing distinct exposure doses. The large polygons have been filled with the same dose, but the interdigitated capacitors differ in dose between them each. Many tests before converging to the best dose and exposure conditions were needed to be applied to each part of the structure. Every test had been reported and discussed, including the improvements or failures achieved. In Annex IV we present exemplary results of some of these tests done.

Summarizing, after several trial and error tests, the whole set of optimum exposure parameters, for a constant return velocity of 0.5mm/s and a focus height of -2.712mm, are as shown in Table 4.1.

| Polygon | Exposure mode | Modulation (%) | Velocity (mm/s) |
|---|---|---|---|
| Connectors (1) | optimized | 50 | 2 |
| Horizontal transmission line (2) | horizontal | 50 | 2 |
| Meander (3) | vertical | 50 | 2 |
| Interdigitated 1+1 capacitor | contour | 25 | 1 |
| Interdigitated 3+2 capacitor | contour | 30 | 1 |

*Table 4.1. Final parameters of lithography for each resonator partition*

With these lithographic values we have accomplished the resonator structure with a required high resolution, patterning accuracy and reproducibility, which have been applied to the resonator fabrication. Importantly, we also have contributed to determine strategies and tested parameters very useful for future works at the IMB-CNM-CSIC and external users of the laser writer.

### 4.5. Experimental results

The achievement of the values in Table 4.1 was not a trivial task. Some experimental work had to be done in order to understand the dependence on the different variables of the laser writer and exposure conditions, and for best accuracy and resolution. For example, Figure 4.8 shows the significant changes in the interdigitated capacitors dimensions when changing the modulation, for a fixed scanning velocity of 1mm/s.

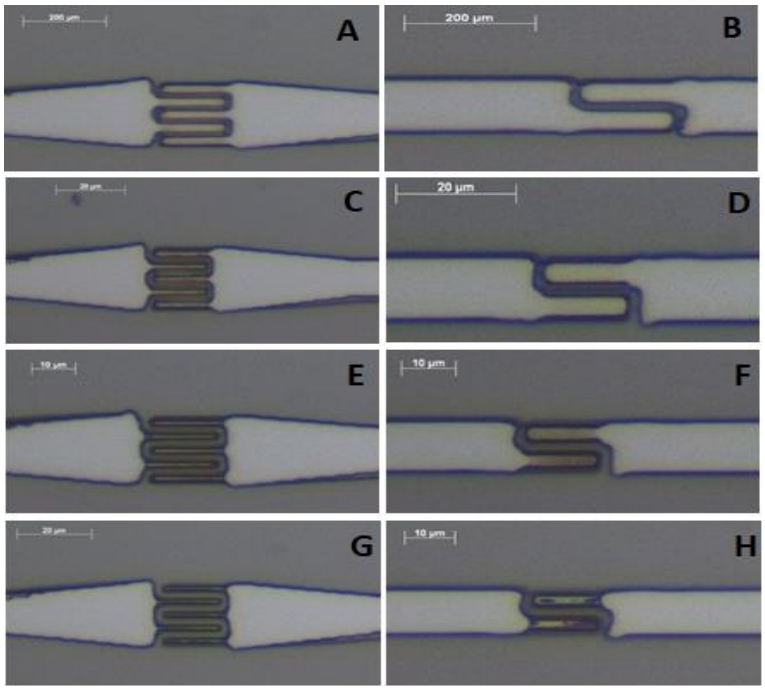


*Figure 4.8. A-B) 3+2 and 1+1 interdigitated capacitor 30% modulation. C-D) 3+2 and 1+1 interdigitated capacitor 25% modulation. E-F) 3+2 and 1+1 interdigitated capacitor 20% modulation. G-H) 3+2 and 1+1 interdigitated capacitor 15% modulation. Fixed scanning velocity of 1mm/s. Optical images.*

The above results exemplify how slight changes on the modulation gives some range for interdigitated capacitors results, for example, for resolving the gaps or realizing nominal values. Looking how the changes in modulation affects the 3+2 interdigitated capacitor (Figure 4.8, A-C-E-G), it is clearly seen, looking the white colour as exposed areas, that increasing modulation is needed to obtain better exposed fingers. Yet, if the modulation increases above 30%, the pattern is overexposed, as it reduces the nominal gap distance to less than 2µm. Inversely, insufficient modulation gives underexposed areas, so the gap will be wider than 2µm and there might be resist rests. Although not fully optimized yet, the 30% modulation value is defined as the upper limit, and best shape accuracy, for the 3+2 interdigitated capacitor. A similar study can be made with the 1+1 interdigitated capacitor (Figures 4.8, B-D-F-H), for which we set 25% modulation as best condition. Accordingly, both values are introduced as the optimized exposure parameters in Table 4.1. The result of applying them simultaneously is shown in the following Figures 4.9-4.11.

### 4.5.1. Pattern transfer

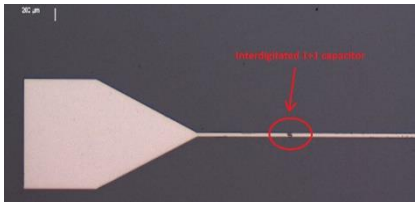

*Figure 4.9. Right connector after lift-off (200µm scale length, with 1+1 interdigitated capacitor (not seen due magnification scale))*

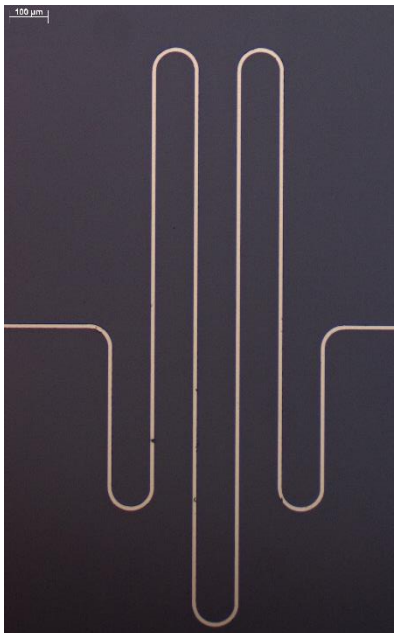

*Figure 4.10. Meander after lift-off (100µm scale length)*

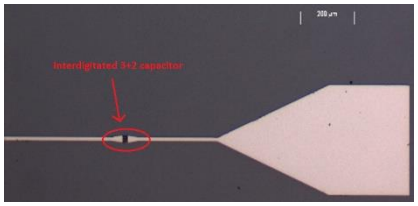

*Figure 4.11. Left connector after lift-off (200µm scale length, with 3+2 interdigitated capacitor (not seen due magnification scale))*

Remarkably, these optimal exposure parameters have not only been validated on the resist, but their pattern transfer by thin metal film deposition and lift of the resist corroborates them. The Figures 4.9-4.11 are the results of the pattern transfer, the whole procedure corresponds to steps detailed in Figure 4.1 (right-side) and the photolithography procedure as introduced in Annex III. Checking each element and part in detail (Figure 4.8), we can conclude that the fabricated resonator agrees well with the nominal dimensions and shape as designed.

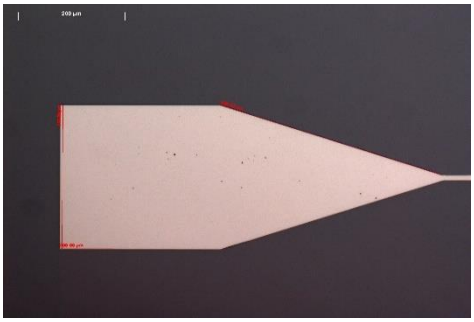

*Figure 4.12. Right connector measurements after lift-off (200µm scale length, 299.99x299.98µm² and 440.82µm slope)*

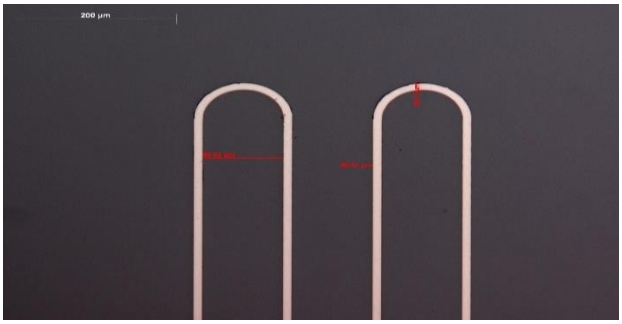


*Figure 4.13. Meander measurements after lift-off (200µm scale length, 99.32µm meander separation and 10.17µm TL width)*

Precisely, from Figures 4.12 and 4.13, we can estimate that the sizes defined in the design correspond to the ones obtained with the pattern transfer. Even if large elements are not so critical, the patterned right-side connector, as well as the left-side one, fits perfectly with its theorical dimensions: 299.99x299.98µm$^2$. The slope is also accurate with respect the desired shape. More challenging elements, if we estimate dimensions in the meander shapes, they are separated 99.32µm while 10.12µm width, which also is in good agree with the parameters of the design.

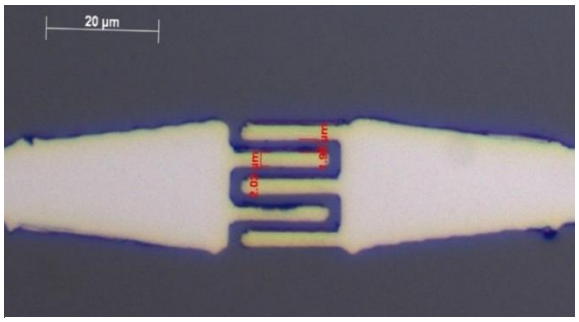


*Figure 4.14. 3+2 interdigitated capacitor after lift-off (20µm scale length, 2.02µm finger width* and 1.96µm gap)

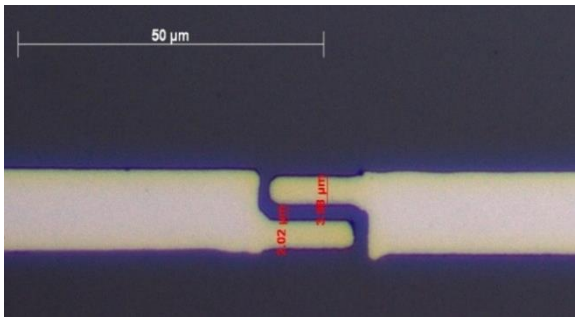


*Figure 4.15. 1+1 Interdigitated capacitor after lift-off (50µm scale length, 3.98µm finger width* and 2.02µm gap)

If we now inspect the critical parts, i.e. the interdigitated capacitors due their finger small size and elements separation, they fully agree with the designed dimensions. The 3+2 interdigitated capacitor, Figure 4.14, can be estimated as in size: 1.96µm interfinger gap and 2.02µm finger width. The line width is basically uniform along the whole finger and edges are significantly well-defined, while the slope and transition with the TL is very clean as well. Similarly, good values are obtained for the 1+1 interdigitated capacitor sizes, see Figure 4.15. The finger gap is estimated as 2.02µm and its width 3.98µm.

While we can finally conclude that the fabricated resonator shown above is very accurate, consistent in dimensions and shape compared with the resonator design, definite prove would be a performance test as an operational resonator. Further work would be checking pattern reproducibility, as we have experienced that unexpected issues can often occur. Some of the different troubles, which we faced, together with solutions that have been implemented, respectively, are detailed in Annex V.

## 5. Conclusions and outlook

In this manuscript, the definition, simulation, design and fabrication of a CPW resonator to be coupled to a superconducting qubit have been presented.

Firstly, by analysing and giving numerical values to the theoretical expression of the transmission line (TL) model, the suitable resonator was designed. Comparing TL theory and the equivalent circuit for harmonic resonators, the parameters needed to obtain a high-quality quality factor ($Q \simeq 10^5$) resonator, for future applications in quantum computing, were extracted. Then, in order to get a first idea of how the resonator would behave in a real environment, its simulation in a 3D simulator, the so-called Sonnet software, was implemented. By designing the resonator operating at a resonant frequency of 7GHz, its resultant transmission spectrum $S_{21}$ was analysed. Despite not achieving the targeted high-quality factor, the resonant frequency and its shift due to the capacitive coupling were correctly fitted with the theoretical predictions. Accordingly, the initial the goal has been redefined as checking the agreement between designing parameters and resonant frequency of the device, which also is reflected in the experimental works as follows.

Experimentally, while accordingly to the literature, and originally the first option, was to fabricate the CPW geometry of the resonator by combining lithography and etching lithographic procedure, both the issue described above, and technical availability made it change. The final fabrication process which best agreed with the new project requirements was lithography followed by metal deposition and lift-off of the resist. Well established materials for this kind of quantum application and experimental conditions are, a metal layer made of aluminium, with appropriate superconductivity properties, and silicon as substrate, which are very well supported by IMB-CNM-CSIC technical capabilities and experience. Yet, for flexible design we have the challenge to use a new direct writing lithography equipment, the laser writer. The so-called Dilase 650 laser writer had recently been installed at the IMB-CNM-CSIC, so the whole procedure and exposure conditions needed to be tested. Additionally, our design was complex and demanding in terms of resolution, actually close to the equipment maximum resolution. Actually, resolution is roughly estimated as 1µm, which is close to the minimum sizes found of the resonator design, i.e. in the capacitor elements.

Despite all these challenges, and as the main conclusion, an aluminium harmonic resonator structure was possible to be fabricated. It presents excellent consistency with the sizes defined in the design.

As some specific studies and developments to continue this work, the following actions are proposed.

- Addressing the problem encountered with Sonnet software simulations by asking recommendations from other technicians more experimented in the field.

- Consolidating the whole laser lithography protocol, to make it fully reproducible and increase chances for fabrication of resonator devices. For instance, some troubles with the photoresist adhesion affected the throughput of the patterning. A recent improvement test included using a primer (HDMS) to reinforce adhesion giving very positive results (see Annex V).

- Experimentally proving that the performance of a fabricated resonator is consistent with its theoretical resonant frequency by measuring at millikelvin temperatures at the ICN2 refrigerator. And then, to evaluate how good are the devices, for targeted quantum computing and simulation applications, and to eventually define a second generation of fully-domestic resonator fabrication suitable for quantum applications.

- Starting the original, alternative technology, i.e. the development based in etching for lithography pattern transfer. Now that we are more familiar with the laser writer preparations and provided that suitable exposure parameters have mostly been established, setting recipes for controlled, high precision etching of the thin Al film, e.g. by the reactive ion etching technique, can be addressed.

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**ANNEX I**

## AI.1. Transmission line theory

The TL model [16] brings us the basis to explain the main element in this study: the solution of the resonator circuit. The phenomenon of wave propagation on transmission lines can be approached as an extension of circuit theory or from specialized of Maxwell's equations.

### A1.1. Using the lumped-element circuit model for a transmission line

A TL can be modelled as a two-wire line system, consisting in two conductors of length Δz. We can model the lumped-element equivalent circuit with some basic circuit components as represented in Figure AI.1, where:

R= series resistance per unit length, for both conductors, in Ω/m.

L= series inductances per unit length, for both conductors, in H/m.

G= shunt conductance per unit length, in S/m.

C= shunt capacitance per unit length, in F/m.

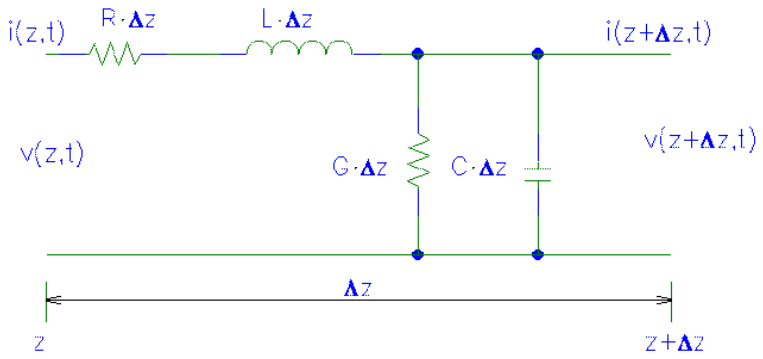



*Figure AI.1. Lumped-element equivalent circuit. Extracted from [28]*

From circuit theory we know that the series inductance L represents the total self-inductance of the two conductors, the shunt capacitance C is due to the proximity of the conductors, the series resistance R represents the resistance due to the finite conductivity of the conductors and the shunt conductance G is due to dielectric loss in the material between the conductors [16]. The two las components account for circuit losses.

Based on circuit of Figure AI.1, Kirchhoff's voltage and current laws can be applied to give the following two expressions.

$$v(z,t) - R\Delta z i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0, \quad \text{(AI.1)}$$

$$i(z,t) - G\Delta z v(z+\Delta z,t) - C\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0. \quad \text{(AI.2)}$$

Dividing both equations by $\Delta z$ and taking the limit as $\Delta z \to 0$, gives the following differential equations, which are the time-domain form for the transmission line equations, by the sinusoidal steady-state condition with cosine-based phasors.

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \rightarrow \frac{dv(z)}{\partial z} = -(R + jwL)I(z) \quad \text{(AI.3)}$$

$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \rightarrow \frac{dI(z)}{\partial z} = -(G + jwC)V(z) \quad \text{(AI.4)}$$

**AI.1.2. Wave propagation in a transmission line**

Now we can compute wave equations for voltage V(z) and current I(z) solving simultaneously the general equations, to obtain,

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0, \quad \text{(AI.5)}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0, \quad \text{(AI.6)}$$

where $\gamma = \alpha + j\beta = \sqrt{(R + jwL)(G + jwC)}$ is the complex propagation constant, a frequency dependent parameter. Travelling wave can now be solved as,

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}, \quad \text{(AI.7)}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}, \quad \text{(AI.8)}$$

where the negative exponential term represents a wave travelling in the +z direction, and the positive term wave propagation in the -z direction. Solving the general equations, the total current in the line is

$$I(z) = \frac{\gamma}{R + jwL}[V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}]. \quad \text{(AI.9)}$$

Now we can define a new term called characteristic impedance $Z_0$, that connects the voltage and current in the line as

$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} = \frac{R + jwL}{\gamma} = \sqrt{\frac{R + jwL}{G + jwC}}, \quad \text{(AI.10)}$$

An expression that relates the current and the impedance can be finally determined,

$$I(z) = \frac{V_0^+}{Z_0} e^{-\gamma z} - \frac{V_0^-}{Z_0} e^{\gamma z}. \quad \text{(AI.11)}$$

### AI.1.3. The lossless transmission line

Expression AI.11 is a general solution and describes any transmission line, including loss effects, in which the propagation constant and characteristic impedance are complex numbers. In many practical cases, however, the loss of the line is very small, and can therefore be neglected, which results in a simplification of the expressions. Given R=G=0 [16] implies that the propagation constant is:

$$\gamma = \alpha + j\beta = jw\sqrt{LC}, \tag{AI.12}$$

where $\beta = w\sqrt{LC}$ and $\alpha = 0$.

We notice, as expected, that in the lossless case the attenuation constant α is zero. Additionally, we can simplify the impedance expression as

$$Z_0 = \sqrt{\frac{L}{C}}, \tag{AI.13}$$

which is a real number. Consequently, the general solutions for voltage and current on a lossless transmission line can then be written as

$$V(z) = V_0^+ e^{-j\beta z} + V_0^- e^{j\beta z}, \tag{AI.14}$$

$$I(z) = \frac{V_0^+}{Z_0} e^{-j\beta z} - \frac{V_0^-}{Z_0} e^{j\beta z}. \tag{AI.15}$$

The wavelength is given by

$$\lambda = \frac{2\pi}{\beta} = \frac{2\pi}{w\sqrt{LC}}, \tag{AI.16}$$

where the phase velocity is

$$v_{ph} = \frac{w}{\beta} = \frac{1}{\sqrt{LC}}. \tag{AI.17}$$

This set of expressions will be basic for a good understanding of the resonator behaviour, based on their characteristic values.

### 1.4. The terminated lossless transmission line

In this section, we will discuss the case of a lossless transmission line terminated in an arbitrary load impedance $Z_L$. In figure AI.2, we assume that an incident wave is injected from some source at z<0. We have seen that the voltage to current ratio for such traveling wave is $Z_0$, the characteristic impedance. But when the line is terminated in an arbitrary load ($Z_L \neq Z_0$), the voltage to current ratio at the load must becomes $Z_L$ [28], [16].

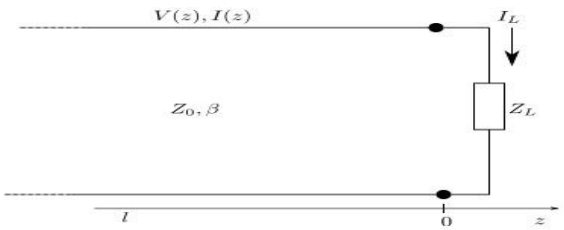



*Figure AI.2. A transmission line terminated in a load impedance. Extracted from [16]*

Thus, a reflected wave needs to be excited with an appropriate amplitude to satisfy this condition. The total voltage and current at the load are linked by the load impedance, so at z=0 we must have

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_0^+ + V_0^-}{V_0^+ - V_0^-} - Z_0. \tag{AI.18}$$

The amplitude of the reflected voltage wave normalized to the amplitude of the incident voltage wave is known as the voltage reflection coefficient, Γ,

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{AI.19}$$

In consequence, the total voltage and current waves of the line can be written as,

$$V(z) = V_0^+[e^{-j\beta z} + \Gamma e^{j\beta z}] \tag{AI.20}$$

$$I(z) = \frac{V_0^+}{Z_0}[e^{-j\beta z} - \Gamma e^{j\beta z}] \tag{AI.21}$$

From these equations it can be observed that the voltage and current on the line consist on a superposition of an incident and a reflected wave; such waves are called standing waves. Only when $\Gamma = 0$ there is no reflected wave. To obtain zero reflection the load impedance $Z_L$ must be equal to the characteristic impedance, $Z_0$, and load is said to be matched to the line; there is no reflection of the incident wave and maximum power is delivered to the load. This real power flowing in the line is constant but the voltage amplitude varies with its position on the line. Therefore, the impedance into the line must vary with position as

$$Z_{in} = \frac{V(-l)}{I(-l)} = Z_0 \frac{V_0^+[e^{j\beta l} + \Gamma e^{-j\beta l}]}{V_0^+[e^{j\beta l} - \Gamma e^{-j\beta l}]} = Z_0 \frac{1 + \Gamma e^{-2j\beta l}}{1 - \Gamma e^{-2j\beta l}} = Z_0 \frac{(Z_L + Z_0)e^{j\beta l} + (Z_L - Z_0)e^{-j\beta l}}{(Z_L + Z_0)e^{j\beta l} - (Z_L - Z_0)e^{-j\beta l}} =$$

$$= Z_0 \frac{Z_L cos\beta l + jZ_0 sin\beta l}{Z_0 cos\beta l + jZ_L sin\beta l} = Z_0 \frac{Z_L + jZ_0 tan\beta l}{Z_0 + jZ_L tan\beta l} \tag{AI.22}$$

**ANNEX II**

### AII.1. Capacitors simulation

Using the analytical expressions of section *"3.1.3. Equivalent resonant circuit",* we obtained the capacitance values (Ck) for the asymmetric coupling capacitors corresponding to a loaded quality factor around $10^5$. Together with the theoretical values, we must define the geometry of the capacitors to be used in the simulation. Sonnet software [30] simulations allows us to design different geometries and obtain a plot of the capacitance as a function of the frequency. The obtained geometries shapes and their respective response are shown in table AII.1.

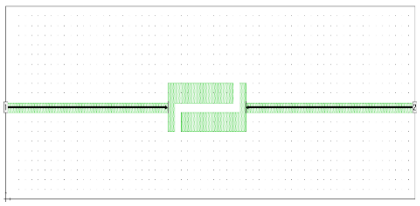
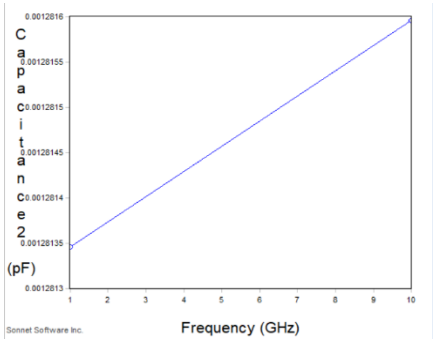
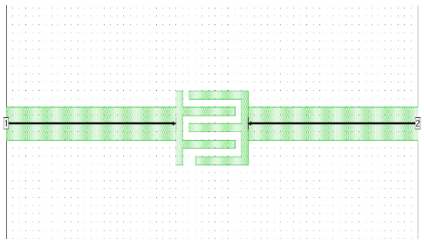
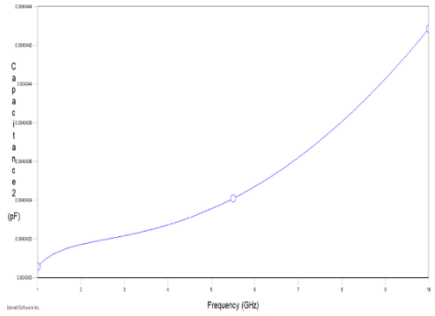
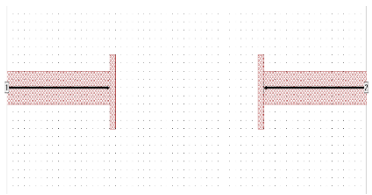
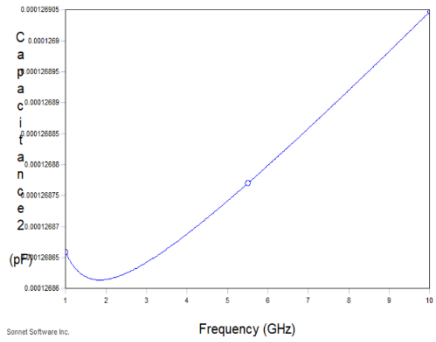
| Capacitance, Ck (fF) | Geometry (# of fingers) | Capacitance (pF) vs frequency (GHz) |
|---|---|---|
| 1.28 | Interdigitation (1+1)  |   |
| 4.04 | Interdigitation (3+2)  |   |
| 0.12 | Parallel 50µm gap  |   |

*Table AII.1. Capacitance, geometry and response of the asymmetric coupling capacitors and the parallel capacitor*

The parallel capacitor geometry was used to simulate the first swept of the device response presented in figure 3.7 from section *"3.2.2. Resonator design"*. For the interdigitated capacitors, their dimensions are showed in table AII.2.

| Geometry | Finger width (µm) | Finger gap (µm) | Finger length (µm) | Height (µm) |
|---|---|---|---|---|
| interdigitated 1+1 | 4 | 2 | 18 | 10 |
| interdigitated 3+2 | 2 | 2 | 16 | 18 |

*Table AII.1. Capacitor dimensions*

In terms of maintaining the characteristic impedance $Z_0$ of the transmission line to match 50Ω, we observe that the height of the interdigitated capacitor 1+1 has to be coincidental with the width of the transmission line (10µm), so that no reflection occurs. On the other hand, as the interdigitated capacitor 3+2 is forcedly wider than the transmission line (18µm >10µm), the connection has to be fit. A solution to keep the condition $Z_0 = 50\Omega$ is to compensate the height misfit with a slope, one that is long enough to avoid any power reflection. This solution is similar to the one explained for the connectors (section "3.*2.2 resonator design").* Supported by the microwave engineering literature [16], we can determine the slope value needed. The final geometry for the interdigitated 3+2 capacitor interdigitated in the TL is shown in figure AII.1.

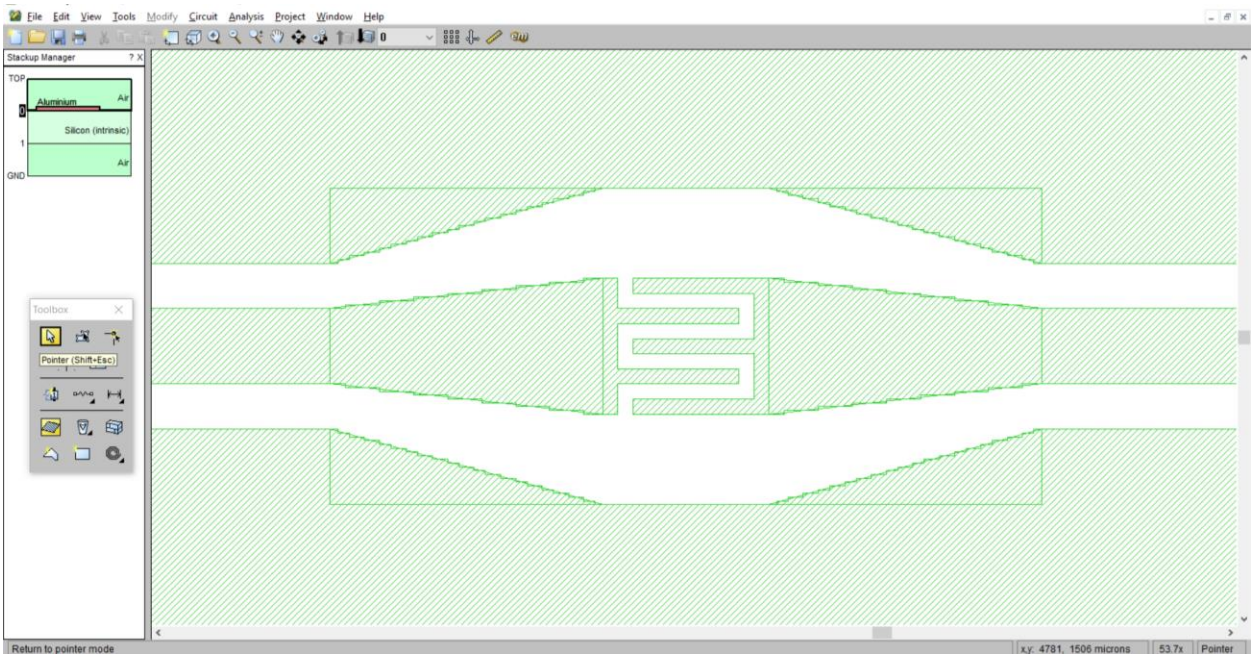



*Figure AII.1. Interdigitated 3+2 capacitor design with slope connecting the transmission line and the capacitor.*

**AII.2. Scattering parameters**

Sonnet software [30] simulations are based on considering a multiport network characterization that can be described by a set of scattering parameters [16], [28]. The complex voltage amplitudes $V_i^-$ of waves originating from port *i,* are tied to the amplitudes $V_j^+$, which are incident on network port *j.* Their relation is expressed as the scattering matrix S, as via $V_i^- = S_{ij}V_j^+$. Matrix elements $S_{ij}$ are found by measuring $V_i^+$ while driving $V_j^-$ and making sure that there are no incident waves on the other ports. Thus defined, their ratio implies that waves originating from the other ports must not be reflected back to the port, which can be realized by terminating them with matched loads. In our case of a two-ports network, the scattering matrix is:

$$\begin{pmatrix} V_1^- \\ \overline{V_2^-} \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} V_1^+ \\ \overline{V_2^+} \end{pmatrix}, \tag{AII.1}$$

where $S_{11} = S_{22}$, the reflection of coefficients at port 1 ($S_{11}$) and 2 ($S_{22}$), and $S_{21} = S_{12}$, for the transmission coefficients from port 1 ($S_{12}$) to 2 ($S_{12}$) and vice versa

Our theorical models are usually formulated in terms of impedance, but the measurement equipment typically displays the S parameters. In the case of two-port networks, the conversion from Z to S corresponds to [16],

$$S_{11} = [(Z_{11} - Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}]/\Delta Z \tag{AII.2}$$

$$S_{21} = \frac{2Z_{12}Z_0}{\Delta Z} \tag{AII.3}$$

$$S_{21} = 2Z_{21}Z_0/\Delta Z \tag{AII.4}$$

$$S_{22} = [(Z_{11} - Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}]/\Delta Z \tag{AII.5}$$

$$\Delta Z = [(Z_{11} - Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}] \tag{AII.6}$$

where

$$S_{11} = S_{22}, \tag{AII.7}$$

$$S_{21} = S_{21}. \tag{AII.8}$$

**ANNEX III**

### AIII.1. Photolithography process

Photolithography [15] is the fundamental and most critical process in the semiconductors industry. It is the basic step for transferring a desired pattern to the surface of a wafer. Ultraclean conditions must be maintained during the lithography process. Any dust particles on the original substrate or that are accidentally deposited on the substrate during manipulation and processing can result in serious defects or complete failure in the final devices or circuits. To minimize risks, vertical laminar-flow hoods in clean room facilities are used to prevent particulate contamination from the air. Clean room facilities are rated by the maximum number of particles per cubic meter on air.

All the fabrication procedures in present work had been done in the clean room of the IMB-CNM-CSIC. Its lithography corresponds to a Class 100 in the rating by Class of Effectiveness of Filtration. Those conditions assure a maximum number, of 0.5µm and 5µm particles size per $m^3$, to, respectively, 3500 and 230. Photolithography is not only exposing the substrate to a light source using a mask, but involves a number of steps. The procedure (process flow) we have applied is schematically presented in Figure AIII.1. Subsequently, each step and procedures are briefly explained including applied experimental examples.

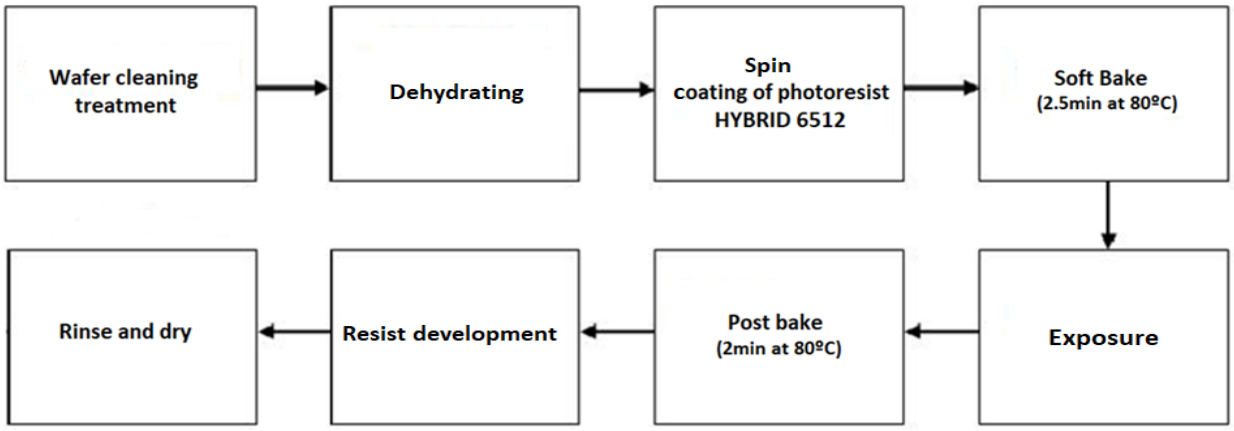



*Figure AIII.1. Steps of the photolithographic process*

#### AIII.1.1. Wafer preparation. Cleaning and dehydrating

Even if silicon wafers used in the clean room are ultraclean as they are received and kept clean from the maker, prior to use, wafers are preconditioned. They are chemically cleaned to remove eventual particulate matter on the surface. We are not processing whole wafers for our tests, so after cutting 4'' silicon wafer in chips of approximately ±1.5$cm^2$ in size, we followed this standard cleaning process:

1. Immersion in electronic grade acetone for 5min to clean the surface from organic contaminants. Usually we add ultrasounds to the treatment for an optimized cleaning.
2. Immersion in electronic grade isopropanol for 5min to remove the remaining acetone rests.
3. Rinsing in deionized water for 1min.
4. Drying with $N_2$ gun.

### AIII.1.2. Photoresist deposition. Spin coating

After the cleaning process, the surface of the Silicon wafer is coated with an ultraviolet (UV) light-sensitive material called photoresist. It is vital to work in an environment with UV filters to avoid undesired resist exposition. The substrate surface must be dry to ensure good photoresist adhesion, so we put the wafer on the hot plate (or oven) at 150ºC for 10min to evaporate any water molecules or solvent.

The photoresist is typically applied in a liquid form, polymer is dissolved on a certain solvent. In our case we have used one of the standard resists used at the IMB-CNM-CSIC, the *HYBRID 6512* positive tone resist. We will later present the meaning of positive and negative resists. The wafer/chip is placed in the spinner *Delta 20 FLI8*, held by a vacuum chuck and, once chosen photoresist has been poured on the substrate, it is spun at high speeds. Particularly, we used a total time of 1.5min and 5 steps with spin velocities in the range of 1000-5000rpm, results in a thin uniform layer of 1.4µm in thickness. The actual thickness of the resist depends on its viscosity and is inversely proportional to the square root of the spinning speed. Typically, resist providers also provide calibration tables according to spin coating conditions.

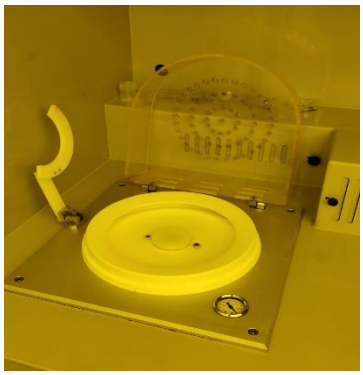


*Figure AIII.2. Delta 20 FLI8 spinner*

*Figure AIII.3. HYBRID 6512 photoresist*

### AIII.1.3. Soft Baking

A thermal heating step called soft baking or prebaking is used to improve adhesion with the substrate and remove solvent rests in the photoresist. The soft-baking process is also specified on the resist manufacturer's data sheet and should be followed closely. For the *HYBRID 6512* resist the wafer must be baked for 2.5min at 80ºC. At this point, the photoresist is ready for the exposure.

*Figure AIII.4. Clean room hot plate*

### AIII.1.4. Photoresist exposure and development

Any positive resist which has been exposed enough to ultraviolet light is washed away when immersed to the appropriate solvent. If exposure is selective, i.e. using a mask, bare silicon will be seen in the selectively exposed areas, and a copy of the pattern will be defined on the surface of the wafer [15]. Inversely, a negative photoresist is hardened, remains, on the surface wherever it has been exposed. *HYBRID 6512* behave like a positive resist. Figure AIII.5 shows a general diagram of how patterns could be transferred onto a silicon wafer using either positive or negative photoresists.

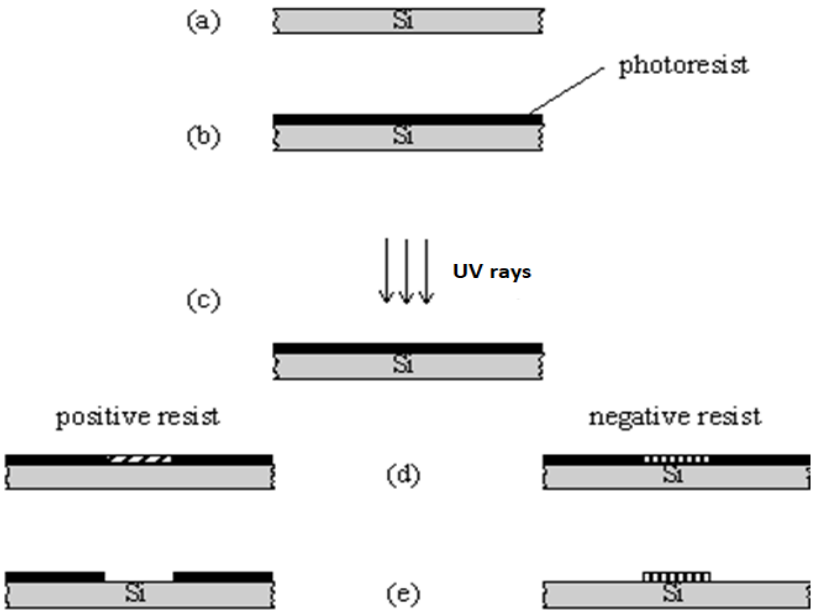



*Figure AIII.5. Resist and silicon patterns following photolithography with positive and negative resists. Extracted from [15]*

The basic chemistry that explains the behaviour of the positive photoresist, which is the component of interest, is simple. *HYBRID 6512* photoresist is an organic polymer which changes its chemical structure when it's exposed at wavelengths in the ultraviolet (UV) spectrum, from 10 to 400nm. It contains a light-sensitive substance whose properties allow image transfer onto a printed circuit board. Some chemical groups of the resist can absorb strongly from UV range, changing their conformation by depolymerization and leading to the zones exposed be more soluble in a suitable developer. Exposed resist is washed away by the developer so that the unexposed areas remains. Light absorption tends to increase with shorter wavelength or larger photon energy.

### AIII.1.5. Hard baking

Following exposure and before development, an additional soft bake step is used to harden the photoresist and promote adhesion to the substrate. The manufacturer's data sheet for the *HYBRID 6512* resist recommend a total time of 2min at 80ºC in a hot plate.

### AIII.1.6. Photoresist development

The last step is to remove the photoresist exposed areas (positive resist) in this case by using the laser beam. The developer used for this purpose is the *OPD 4262*. It uses proprietary-liquid resist strippers, which cause the resist to swell and lose adhesion to the substrate. We must prevent direct contact with the product, which is corrosive, so protection glasses and gloves should be used, as well as laminar flux ventilation. The used photoresist removal protocol used was:

1. Immersion in *OPD 4262* developer for 1min to remove the exposed photoresist.
2. Immersion in a waterfall for 15s to stop the developer reaction.
3. Immersion in distilled water for 15s to remove the remaining developer.
4. Drying with $N_2$ gun.

Inspection has been done on an optic microscope. If the patterning results are good the metallization and lift-off procedure can be proceeded.

### AIII.1.7. Metal deposition

According to defined structure in section 3.1.1.2, 100nm aluminium film has been deposited by a physical deposition technique, Thermal Evaporation. This process is done by specialized engineers which are staff at the IMB-CNM-CSIC clean room.

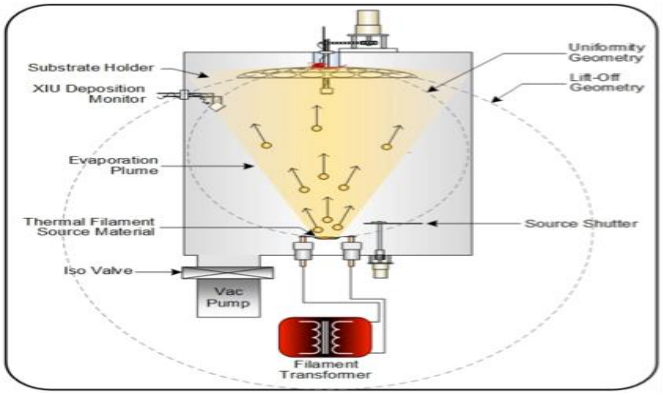



*Figure AIII.6. Physical Thermal Deposition diagram. Extracted from [33]*

The final step of the fabrication, to complete pattern transfer, is the lift-off of the resist. In this step, unexposed and therefore not developed areas are removes, so is the Al covering those areas. The procedure to be applied is similar to the one done for wafer cleaning. Yet, we typically avoid ultrasonication, as the metal films is quite thin, and sometimes stronger chemicals (strippers) have to be applied.

### AIII.2. Laser writer. Equipment description

The Dilase 650 [27] is equipped with a single laser source of wavelength 375nm and two optical paths. Each optical path ensures the optical beam shape to obtain a specific laser spot width. Our system is provided with beam sizes of 1µm and 10µm in diameter. We have also two optical lenses, for each optical line, with x10 and x40 enlargement respectively. Therefore, for our main configuration, the maximum resolution we can attain with the laser writer, after perfectly focusing the device, is 1µm. It is possible to optimize throughput of Dilase 650's performance by appropriately choosing one of the two optical lines, depending on the geometries and the minimal resolution of the elements of the designed patterns.

The equipment is equipped with a set of XY motorized stages that allow accessing a working area of 150mm x 150mm. Movement has a standard nominal positioning accuracy of 100nm. The stage is a flat chuck that holds the sample, by using vacuum, during the writing. The Dilase 650 is equipped with a set of software tools operate the system, e.g. display of the patterns and managing repositioning dedicated to the superposition of lithographic patterns. It is necessary that the position of the pattern is precisely defined, which should be written with the best repositioning accuracies possible, typically attainable with a resolution of about 1µm. For pattern referencing on the sample, it has a optical system composed by a white light source and an optical homogenizing illumination, as well, with a camera sensor. Table AIII.1 contains the maker specifications of the Dilase 650 equipment and figure AIII.7 a general overview of the equipment actual equipment as installed in IMB-CNM-CSIC Clean Room.

| **DILASE 650** | |
|---|---|
| Diode laser wavelength | 375nm |
| Optical line 1: laser spot size after focusing | 1µm (+/-250nm) |
| Optical line 2: laser spot size after focusing | 10µm (+/-250nm) |
| Lens enlargement | X10 or x40 |
| Numerical aperture (N.A.) | 0.13 to 0.95 |

*Table AIII.1. Dilase 650 specifications. Extracted from [27]*


*Figure AIII.7. Overview of the Dilase 650 equipment*

**AIII.3. Operation procedure**

The software suite of the Dilase 650 is composed of two separate applications*: "Kloédesign",* which allows patterns design, simulation; and *"SoftDilase650",* which can control the equipment and performs the automated writing.

As preparation for the laser exposure, we must follow initialization steps of the Dilase 650 software [27], as:

a) Start the equipment by turning ON the start-up key and wait until the start of the machine and the computer station is complete.

b) The equipment is now ready to work, but stage must be initialized. This initialization is started manually using the control software DilaseSoft650 while is active: see stage 1 of figure AIII.8 that shows its general interface. After a short time, the automated mobile chuck starts moving and runs to its original coordinate (0,0,0). Once complete the routine, the initialization of the motors and the focal length will stop, and the interface becomes active.

c) Now we can load the sample into the stage making sure that all the vacuum holes are covered and then activate the vacuum.

d) In stage 4 we have the control panel for the camera system that allows a real-time viewing of the wafer surface. Thanks to this option we can set the origin or reference point (0,0), to define where on the sample the laser will execute the pattern exposures. Moving the motorized stages, we can assign the origin in stage 3. For instance, by convention we use the left bottom corner of the silicon wafer as our reference position.

e) We must adjust the focusing height close to the location to be patterned, a crucial step to get an optimum resolution. Right-side in stage 3 allows controlling the focusing, stage Z motion is chosen to adjust the height. The focusing height depends on the type of photoresist and its thickness, as well as the sample or substrate thickness. For the HYBRID 6512 resin spin coated to provide a 1.4µm thickness, we have a typical focusing height (Zo) of -2.060mm. But this is not our final focus value, we shall add a height form factor (Hf) that is the tolerance for the optical line 1 (for 1µm laser head). Therefore, the optimal focusing height for the resin given is -2.060 – 0.105mm (Zo + Hf). For each experiment we must adjust the focusing height. We have to check the sample planetary as well. Practically, we will move the stage, with the light of the laser head turned on, within the chip surface, for instance, in search of some spot on the top of the resist or substrate reference (such as a scratch or predefined pattern), which we can use to adjust the optimal focusing height. It's important to remember that the photoresist is sensitive to the visible light, so we must adjust the focus as fast as possible and not on the target exposure, in order to not expose the resin.

f) Finally, as stage 6 we will load the pattern design, e.g. resonator, in the form of LWO extension, and define all exposure parameters as well as define the optical line for each of the designs that will be exposed. Automated execution of a group of files is possible in what is so-called position list, which allows specifying the location on the sample for each.

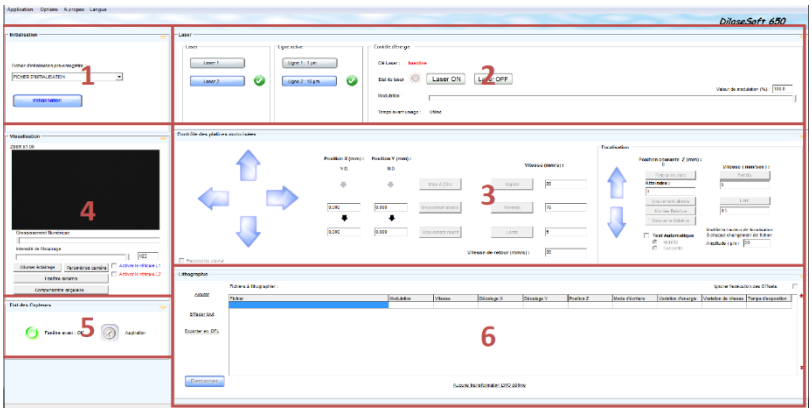



*Figure AIII.8. General interface of the Soft Dilase 650 application. Extracted from [27]*

### AIII.4. LWO files importation

As mwntioned, LWO file is the only readable file type by the equipment Dilase 650. This type of file is generated exclusively with the design software "KloéDesign", which allows to:

- Create, modificate and simulate complex patterns using elementary patterns and accessible from the software library, as straight line, arc of circle and polygon.
- Convert DXF and GDS files to LWO type.

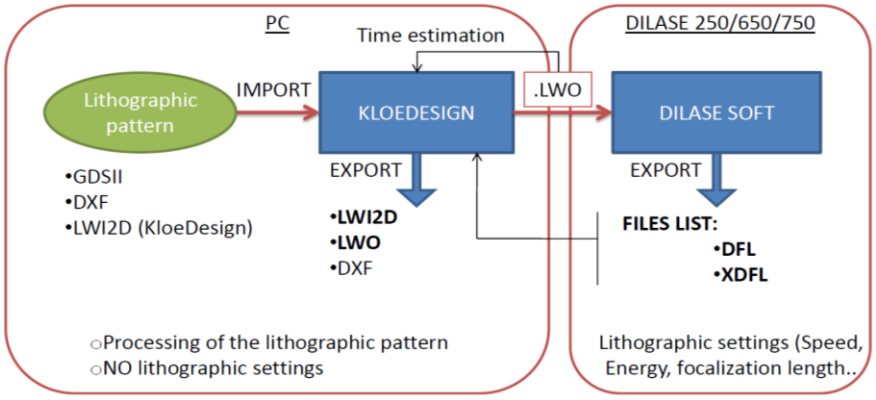



*Figure AIII.9. Kloe software pathway files. Extracted from [27]*

Figure AIII.9 shows the schematic path to obtain the LWO file, which is needed to proceed to execute, expose a pattern. First, we should design our pattern with some a software which allows exporting files such as GDS or DXF files. Secondly, after the GDS file is generated, we can import it in the "KloéDesign" application, where we will define the exposure settings. Finally, the LWO file is generated and added to the table list in the "Dilasesoft650" program, which allows us to set the basic parameters for the exposure.

**ANNEX IV**

**20181127 - Report chip 24**

Five complete resonators structures (different as the ones in the main manuscript) were exposed by using the following conditions.

**Exposure conditions:**

| Design type | Modulation (%) | Velocity (mm/s) | Position on chip X, Y (mm) | Focus Z (mm) | Identifier |
|---|---|---|---|---|---|
| Filling | 40 | 3 | 4, 5 | -2.155 | A |
| Gap | 45 | 3 | 4, 5 | -2.155 | |
| Filling | 40 | 3 | 4, 8 | -2.155 | B |
| Gap | 50 | 3 | 4, 8 | -2.155 | |
| Filling | 40 | 3 | 9, 5 | -2.155 | C |
| Gap | 45 | 2 | 9, 5 | -2.155 | |
| Filling | 40 | 3 | 9, 8 | -2.155 | D |
| Gap | 50 | 2 | 9, 8 | -2.155 | |
| Filling | 40 | 3 | 6.5, 10 | -2.155 | E |
| Gap | 40 | 3 | 6.5, 10 | -2.155 | |

*Table AIV.1. Report chip 24, doses tested*

**Experimental results:**

**A)**

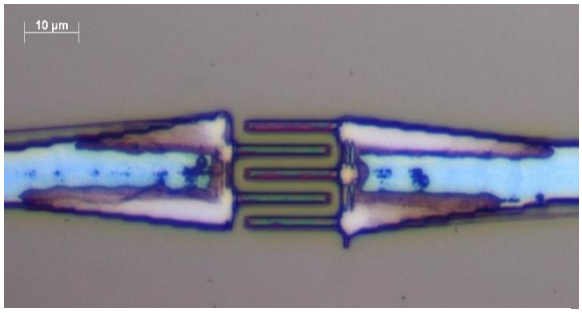



*Figure AIV.1. Interdigitated 3+2 capacitor dose A. Chip 24*

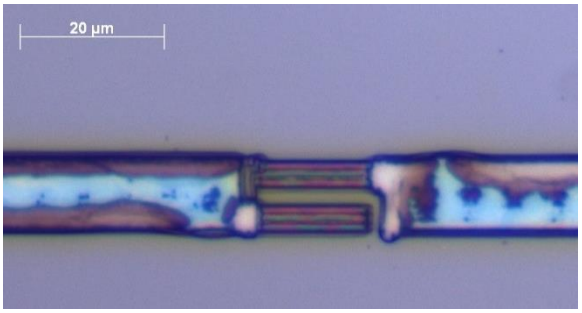



*Figure AIV.2. Interdigitated 1+1 capacitor dose A. Chip 24*

**B)**

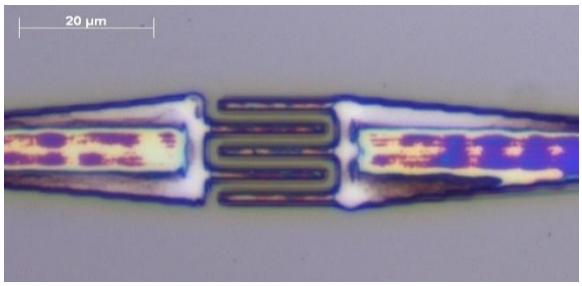



*Figure AIV.3. Interdigitated 3+2 capacitor dose B. Chip 24*

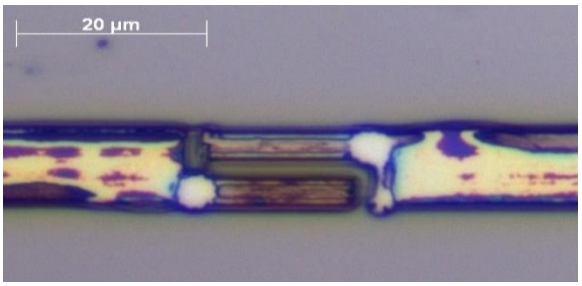



*Figure AIV.4. Interdigitated 1+1 capacitor dose B. Chip 24*

**C)**

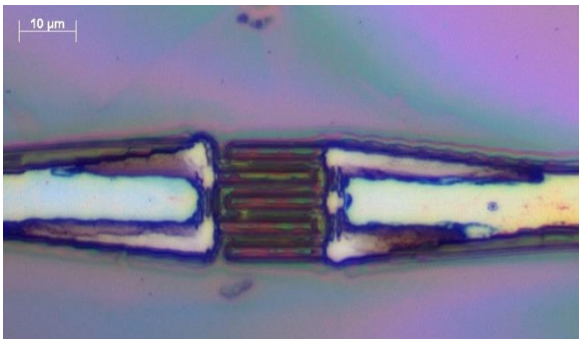



*Figure AIV.5. Interdigitated 3+2 capacitor dose C. Chip 24*

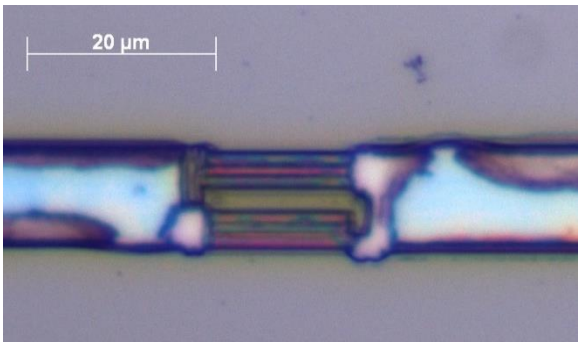



*Figure AIV.6. Interdigitated 1+1 capacitor dose C. Chip 24*

**D)**

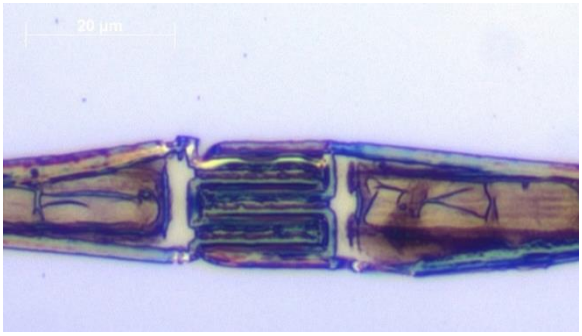
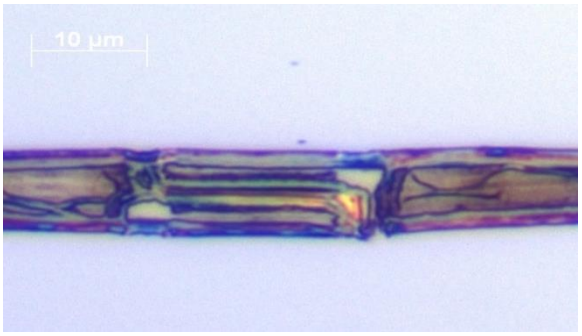



*Figure AIV.7. Interdigitated 3+2 capacitor dose D. Chip 24*




*8Figure AIV.8. Interdigitated 1+1 capacitor dose D. Chip 24*

**E)**

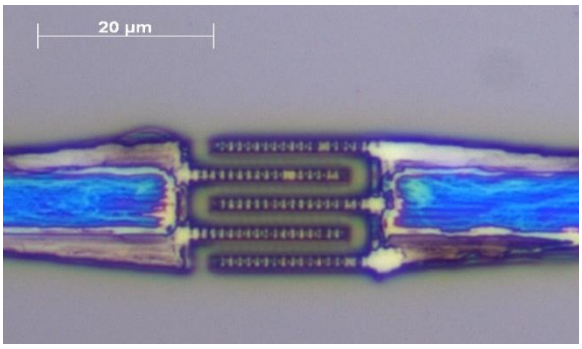



*Figure AIV.9. Interdigitated 3+2 capacitor dose E. Chip 24*

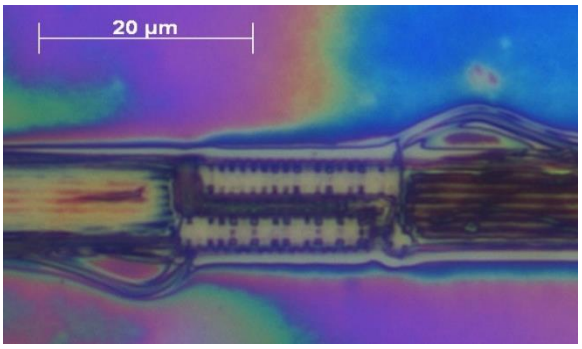



*Figure AIV.10. Interdigitated 1+1 capacitor dose E. Chip 24*

**Comments:**

As we can see from the results of the OM inspection, we can achieve a capacitor with a good definition by the strategic design. For instance, the four first resonators have been designed with horizontal lines and two vertical lines at the edge, where the connector limits. There, we can see some white spots, an indication that the resist has been completely removed (developed) because laser trajectories. It occurs were the laser beam passed twice, in other words, where vertical and horizontal lines cross. Relatedly, filled polygons become not fully developed as the beam was delivered only once. We can observe this effect as colours, corresponding to remaining resist thickness variations.

We attempted to reach removal development by some additional time (10s extra) in the developer unsuccessfully. This means that exposure dose was insufficient. Additionally, we promoted detachment close to or break of the exposed areas (images D and E).

Finally, if we look at image E, we can see another type of gap design, where we have drawn a series of small vertical parallel lines along the longitudinal direction of the transmission line. Thanks to this design we aimed to optimize the exposure of the structure. But, contrarily, we didn't achieve the expected or better definition, because those lines are still seen on the transmission line, so conditions were not adequate.

Based on these results, discarded structure E, while structures A, B, C and D could be used to find optimized results as they closer to the goal. Following figures correspond to strategic design used.

**Outline**

a) A-D, GAP contour:

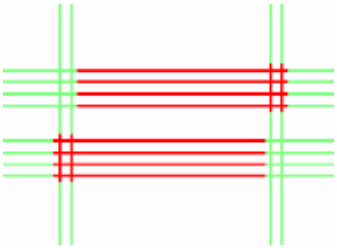


*Figure AIV.11. Laser trajectories of the interdigitated 1+1 capacitor. Chip 24*

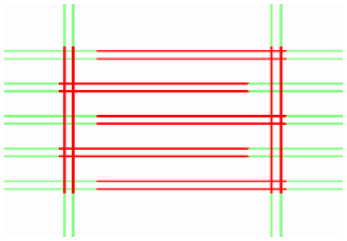


*Figure AIV.12. Laser trajectories of the interdigitated 3+2 capacitor. Chip 24*

b) E, GAP contour:

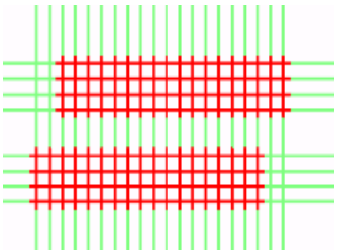


*Figure AIV.13. Laser trajectories of the interdigitated 1+1 capacitor for dose E. Chip 24*

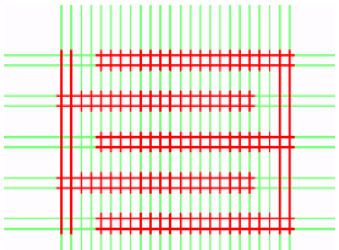


*Figure AIV.14. Laser trajectories of the interdigitated 3+2 capacitor for dose E. Chip 24*

**20181204 – Report chip 26**

Four complete resonators structures (different as the ones in the main manuscript) were exposed by using the following conditions.

**Dose:**

| Design type | Modulation (%) | Velocity (mm/s) | Position on chip X, Y (mm) | Focus Z (mm) | Identifier |
|---|---|---|---|---|---|
| filling | 40 | 3 | 4, 4 | -2,171 | A |
| gap | 40 | 3 | 4, 4 | -2,171 | |
| filling | 40 | 3 | 10, 4 | -2,171 | B |
| gap | 30 | 3 | 10, 4 | -2,171 | |
| filling | 40 | 3 | 4, 8 | -2,171 | C |
| gap | 30 | 1 | 4, 8 | -2,171 | |
| filling | 40 | 3 | 10, 8 | -2,171 | D |
| gap | 20 | 1 | 10, 8 | -2,171 | |

*Table AIV.2. Report chip 26, doses tested*

**Experimental results:**

**A)**

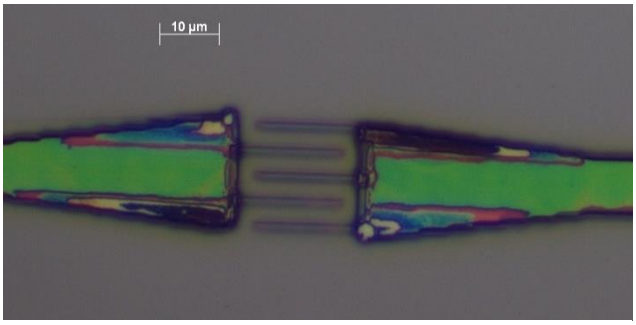



*Figure AIV.15. Interdigitated 3+2 capacitor dose A. Chip 26*

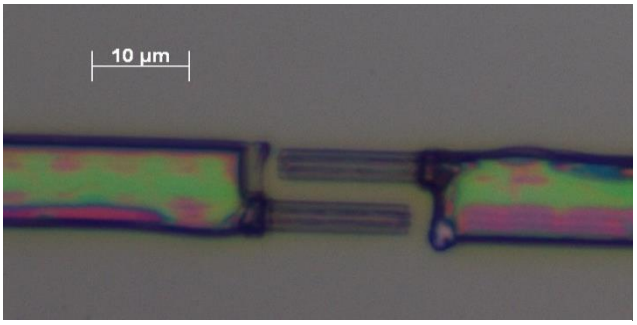



*Figure AIV.16. Interdigitated 1+1 capacitor dose A. Chip 26*

**B)**

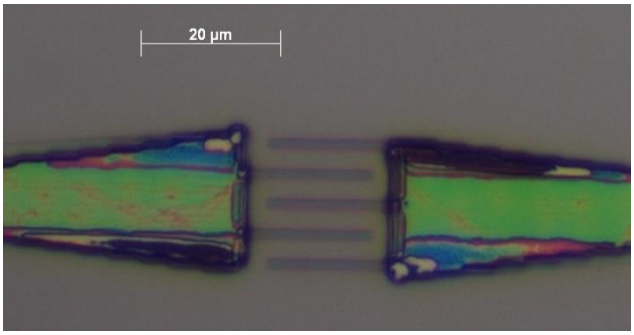



*Figure AIV.17. Interdigitated 3+2 capacitor dose B. Chip 26*

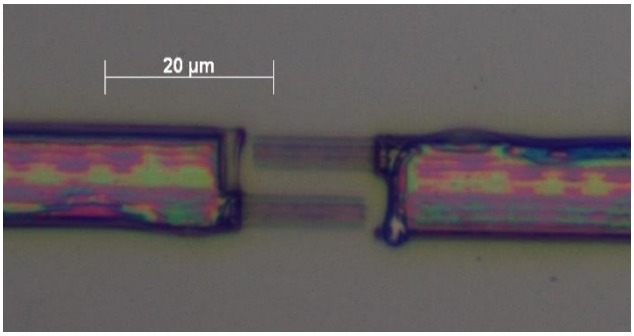



*Figure AIV.18. Interdigitated 1+1 capacitor dose B. Chip 26*

**C)**

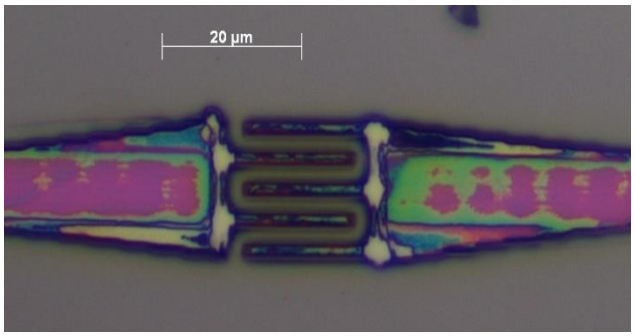



*Figure AIV.19. Interdigitated 3+2 capacitor dose C. Chip 26*

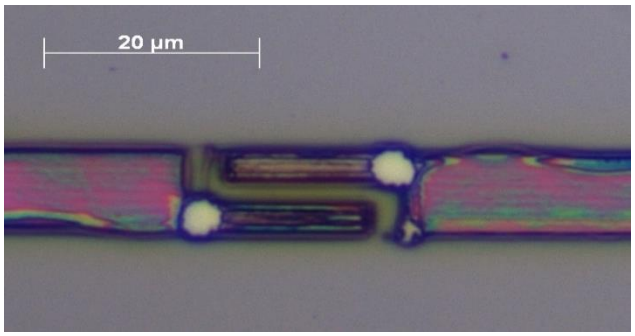



*Figure AIV.20. Interdigitated 1+1 capacitor dose C. Chip 26*

**D)**

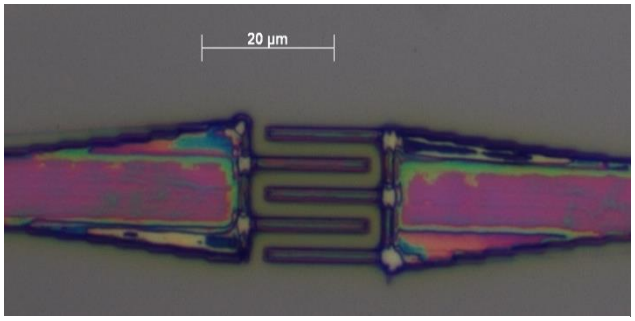



*Figure AIV.21. Interdigitated 3+2 capacitor dose D. Chip 26*

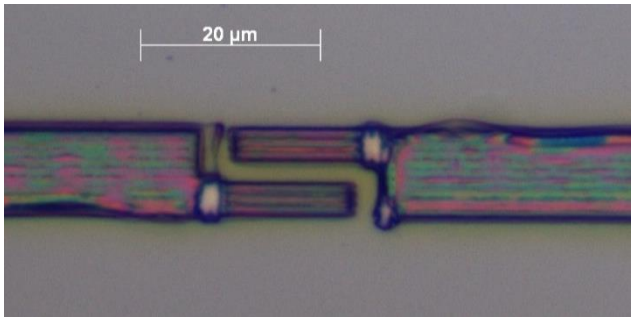



*Figure AIV.22. Interdigitated 1+1 capacitor dose D. Chip 26*

**Other curious results:**

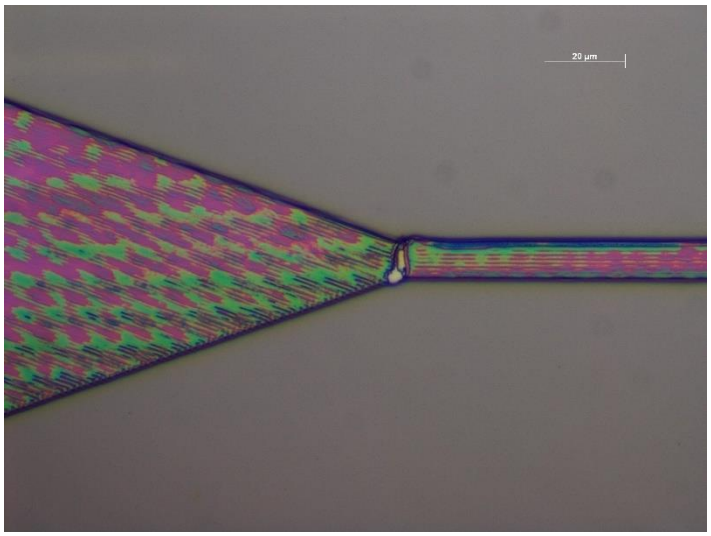


*Figure AIV.23. Left connector on photoresist view*

**Comments:**

That day we did some trials actually very similar to the last test (03/11/2018), we checked a similar range of velocities and modulation, but now we tested two different velocities to explore changes in size. If we look images A and B, we can see the focus height is not well adjusted. This trouble can be caused by a relation between velocity and modulation which is not well matched. Therefore, in future tests we must change one of these values to evaluate if a better resolution and the absolute symmetry in size is possible.

On the other hand, if we take a look on images C and D we can check that we have more resolution than other tests; it seems clear with a slower velocity, 1mm/s, we get more control on the beam delivery, and accordingly we obtain a better symmetry in size and obtain all the structures similarly exposed, with no misfit in colour. From this point we decided that this is the best option to improve the capacitor resolution, changing modulation and fixing velocity. It is also clear that we only get a good exposition when the contour lines appropriately cross. In other words, when vertical and horizontal lines overlaps, we often get full exposure of the resist.

Yet, we must still change some parameters of the filling of the polygons because they are still not as well exposed as we need (actually laser trajectories/direction along the polygons can be clearly identified): maybe reducing the scanning velocity and increasing the modulation can solve our problem (correct exposure dose). To be further investigated next time.

## ANNEX V

### AV.1. Common troubles faced during the setup of the whole fabrication process

- **Over and under photoresist exposure**

Before we have been able to find optimal laser trajectories and good exposure parameters, we have tested several strategies. For example, splitting the resonator into two separates exposure modes was not our initial approach. We had actually begun by exposing the whole resonator only using the filling mode, excluding the contours for the capacitor. The initials laser trajectories used to expose the capacitors are showed in figures AV.1 and AV.2.

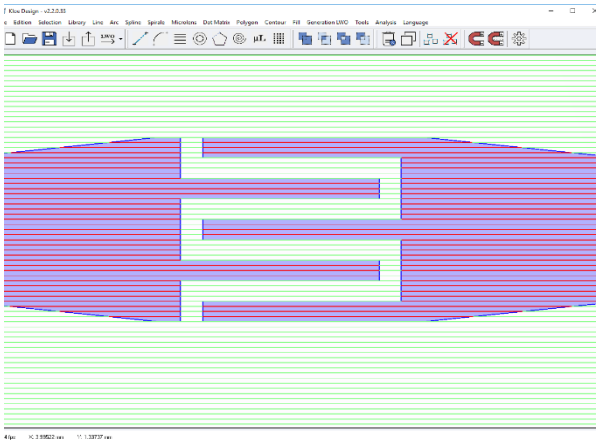


*Figure AV.1. Laser trajectories interdigitated 3+2 capacitor*

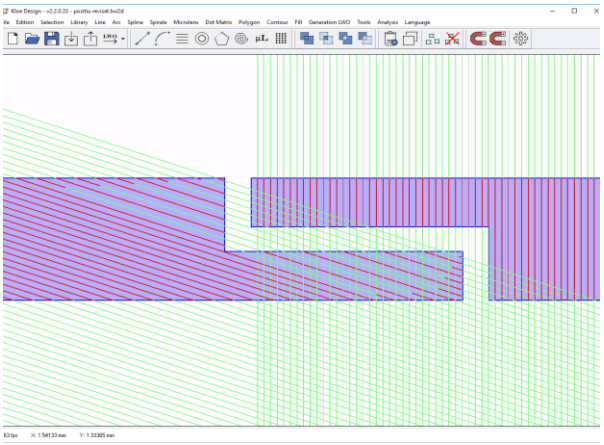


*Figure AV.2. Laser trajectories interdigitated 1+1 capacitor*

The laser trajectories showed above are assumed to have a spot size of 1µm. But we can notice that they do not precisely fit, and therefore, are not evenly distributed along the capacitor's polygons, with no reference coordinate or origin specified. Thus, this strategy does not fit when the dimensions and shape match the trajectories filling periodicity. Experimentall, we get asymmetric fingers and gaps width, with poor patterning accuracy and resolution. Furthermore, the most usual effect that we get is an overexposure of the capacitors, where no finger shape is left. Experimental results of this problem are shown in figures AV.3 and AV.4. On the other hand, we also had underexposed issues linked to beam and trajectories separation. Some examples are showed in Figures AV.5, AV.6 and AV.7.

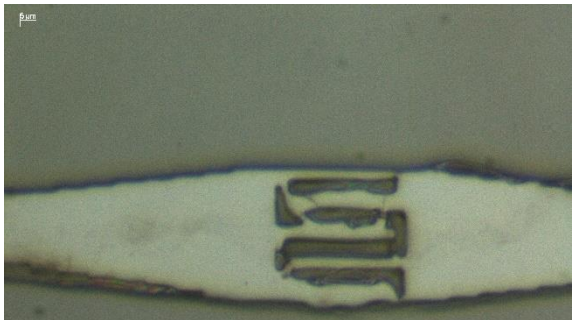


*Figure AV.3. Interdigitated 3+2 capacitor with filling mode*

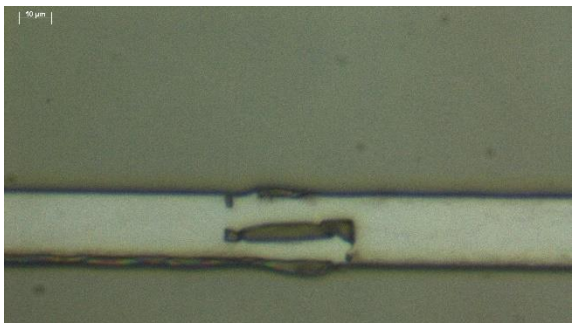


*Figure AV.4. Interdigitated 1+1 capacitor with filling mode*

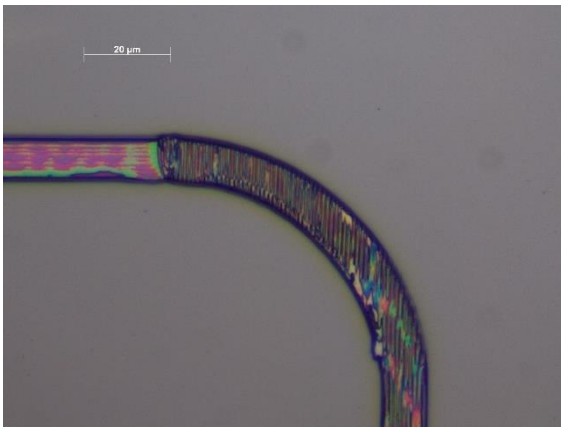



*Figure AV.5. Horizontal and meander transmission line linking underexposed*

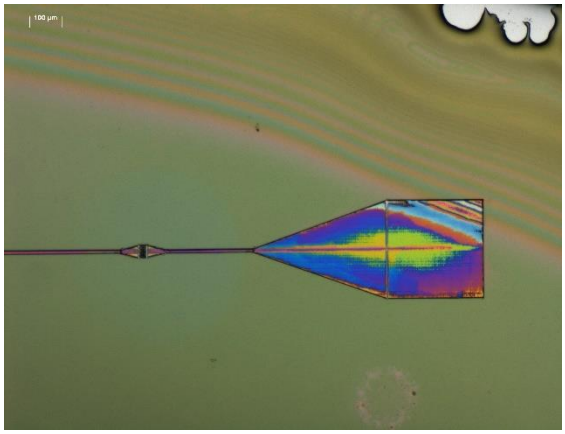



*Figure AV. 6. Right connector underexposed*

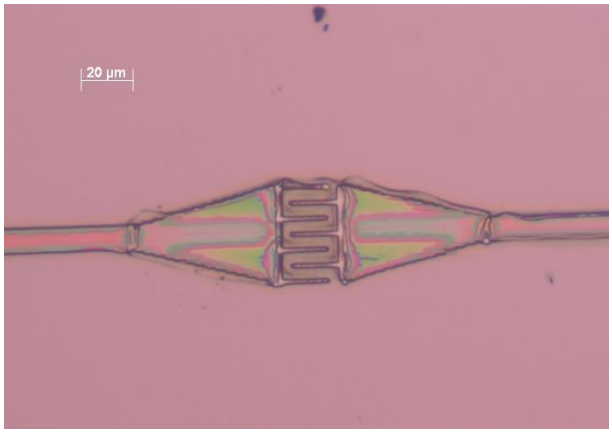



*Figure AV.7. Interdigitated 3+2 capacitor underexposed*

- **Photoresist adhesion**

Sometimes one of the most serious issue is that, we had some photoresist adhesion problems on structures that had very finely patterned. Figures AV.8 and AV.9 shows two examples of resin from the meander area that have detached from the substrate after being exposed to the UV laser beam and developed. We hypothesize the meander shape made them very critical in terms of adhesion, which may be linked to swelling, heating due to their close, serpentine arrangement. We have four vertical transmission lines, separated 100µm from each other, and connected by a half circumference of 50µm radius. This pattern concentration and photoresist stress could be the origin of the poor adhesion around meanders.

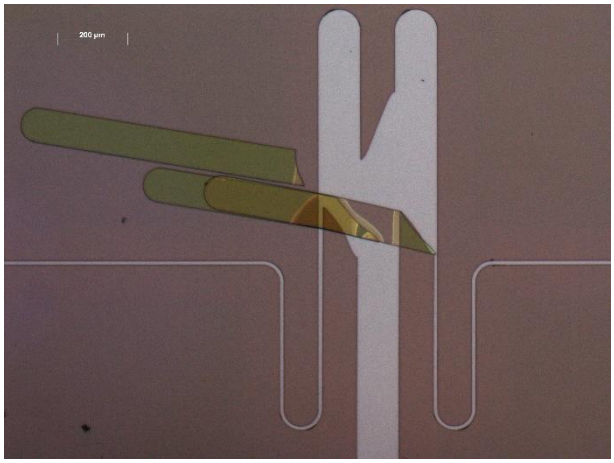


*Figure AV.8. Photoresist adhesion trouble 1*

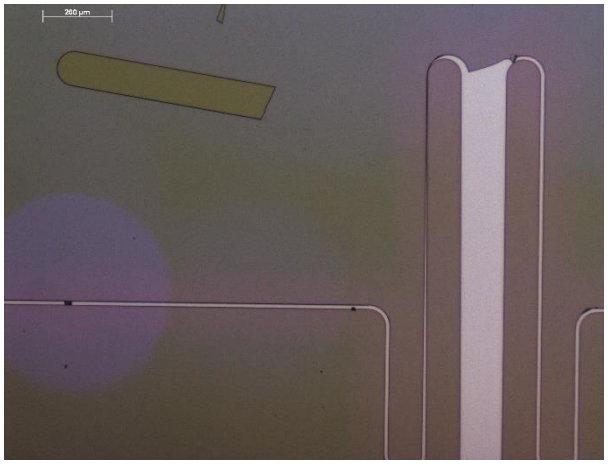


*Figure AV.9. Photoresist adhesion trouble 2*

One possible solution to this issue has been to incorporate the use of a primer in the whole photolithography procedure [32]. A primer is an adhesion promoter, a chemical that improves resist adhesion on substrates such as Si. Usually, it is applied via spin coating, where a sub-mono layer becomes adsorbed onto the surface. Consequently, the surface is said to be activated. One of the most common primers used for this purpose is hexamethyldisilazane (HDMS). The result of laser exposure in a sample applying HDMS is showed in Figure AV.10, which indeed corroborated as a great adhesion improvement.

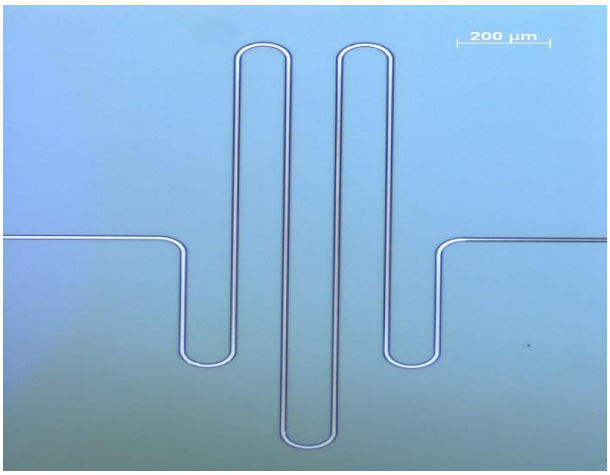



*Figure AV.10. Meander structure over photoresist after using the HDMS primer.*

- **Lift-off resolution**

Another difficulty we experimentally encountered is the lift-off procedure. After the 100µm thickness aluminium deposition and the removing of the parts in contact with the photoresist, there were some metal remaining in unwanted parts of the structure, such as gaps. The finger gaps of the interdigitated capacitors, both of 2µm width, were the zones of the design where we had more difficulties to eliminate the aluminium plus photoresist. No favourable resist profile or rests are among the sources of this phenomenon. If we do not fully eliminate the metal from the gaps, the structure is useless, that is an electrical short-cut would appear. Therefore, sometimes simple cleaning procedure is not enough, and we need using a more aggressive chemical product. To this purpose an additional stripper was used. Figures from AV.11 to AV.14. show the effect of stripper used, which improves fabrication yield.

- **Before stripper**

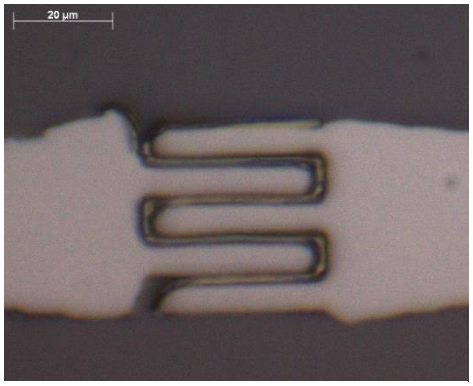



*Figure AV.11. 3+2 interdigitated capacitor before stripper*

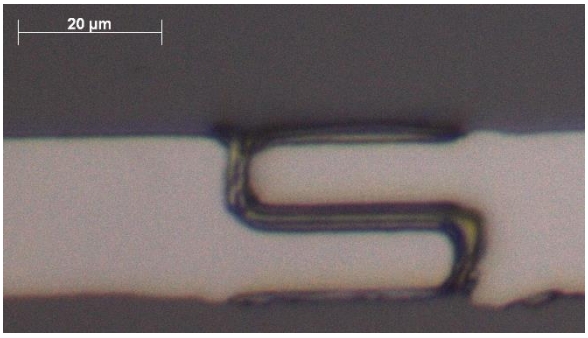



*Figure AV.12 1+1 interdigitated capacitor before stripper*

- **After stripper**

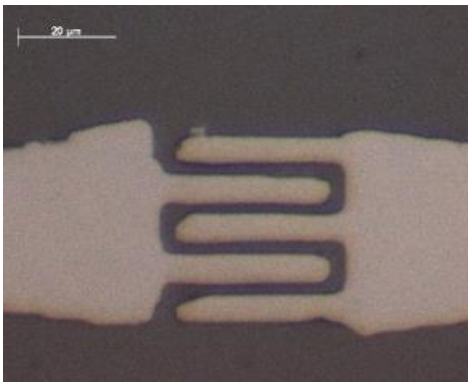


*Figure AV.13. 3+2 interdigitated capacitor after stripper*


*Figure AV.14.1+1 interdigitated capacitor before stripper*

## Acronym and abbreviation list

- **BSC theory**: Bardeen, Cooper and Schrieffer theory
- **QED circuit**: quantum electrodynamics circuit
- **CPW**: coplanar waveguide
- **Qubit:** quantum bit
- **ICN2:** Catalan Institute of Nanotechnology
- **IMB-CNM-CSIC:** Institute of Microelectronics of Barcelona - National Microelectronics Centre – Spanish National Research Council
- **JJ**: Josephson junction
- **MW theory:** Microwave theory
- **OM:** optical microscopy
- **SBCNM**: National Microelectronics Centre Clean Room
- **TL**: transmission line
- **Tc**: critical temperature
- **VNA**: vector network analyser

## Acknowledgements

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