Master's degree: Advanced nanoscience and nanotechnology

Autonomous University of Barcelona (UAB)

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High Energy physics institute (IFAE)

SUPERCONDUCTING COPLANAR WAVEGUIDE RESONATORS FOR QUANTUM COMPUTING

FINAL MASTER PROJECT

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Contents

Acronyms

- MW: Microwave
- TL: Transmission line
- CPW: Coplanar waveguide
- Qubit: quantum bit
- IMB-CNM : Institute of Microelectronics of Barcelona
- IFAE: Insitute for High Energy Physics
- VNA: Vector network analyser
- SEM: Scanning electron microscopy
- GND: Ground
- QED: Quantum electrodynamics
- Z_{in} : Input impedance
- Z_0 : Characteristic impedance
- P_{in}: Input power
- P_{loss} : Power loss
- L : Inductance
- C : Capacitance
- R : Resistance
- R_L : Load resistance
- C_k : Coupling capacitance
- G : Conductance
- I : Current
- V : Voltage
- ω : Angular frequency
- W_e : Electric energy
- W_m : Magnetic energy

- v_{ph} : Phase velocity
- β : Phase constant
- α : Total attenuation
- α_R : Radiative attenuation
- α_C : Metal conductivity attenuation
- α_D : Dielectric attenuation due to loss tangent
- α_G : Dielectric conductivity attenuation
- γ : Complex constant propagation
- l : Length
- f_0 : Resonant frequency
- λ : Wavelength
- Q_{total} : Total quality factor
- Q_{ext} : External quality factor
- Q_{int} : Internal quality factor
- T_c : Critical temperature
- ϵ_0: Vacuum electric permitivity
- ϵ_{eff}: Effective electric permitivity
- μ_0: Vacuum magnetic permeability
- ϵ_{eff}: Effective electric permitivity

Chapter 1

Introduction

1.1 Presentation of topic

The creation of the first classical computers, pioneered by Alan Turing, was a turning point in the history of computation [1]. Turing laid the foundations of what we know today as classical computers, that anyone has in pocket, at home, at work, etc. These devices use processes that follow human logic, based on what is commonly known as a logical state or information bit, that is, ON or OFF, alive or dead, 0 or 1, current or no current (being transistors essential for that purpose). From this basic information, boolean algebra and logical gates can be made, building large and complex computational processors [2].

Trying to reduce the size of the processors, while keeping their computational power, has resulted in an effort to make more efficient devices by decreasing the size of transistors on a nanometric scale [3], to fit inside chips. Such a point has reached where the classical laws begin to fail and quantum description is needed. Quantum bits, or qubits, are the basic unit of quantum information, being quantum mechanical two-level systems that may be in a simultaneous superposition of their basis states [3]. These systems can be created from different physical platforms such as electron spins [4], the polarization of photons [5], or from superconducting circuits[6].

Many discoveries have been made, mainly focused on creating new and much more effective materials, to be implemented in quantum computers [3]. Superconductors are materials that can be used to implement quantum computers [3]. Superconductivity has the property of possessing no electrical resistance to a passing current at a specific critical temperature [7]. These materials are being used in many circuits such as resonators and qubits with Josephson junctions to build quantum processors.

Josephson Junctions (JJ) are electrical circuit elements consisting of two superconducting materials separated by a thin layer of insulator, across which an electrical supercurrent may flow in the absence of a voltage difference [3]. Electron pairs can cross through the insulating barrier by the Josephson tunneling effect [8]. The Josephson effect is influenced by magnetic fields, a capacity that enables the JJ to be used in devices such as SQUIDs (superconducting quantum interference devices) that measure extremely weak magnetic fields [9]. JJ have been used in many applications for qubits [10, 11], being very attractive due to low dissipation and high nonlinearity. JJ can be fabricated using integrated-circuit processing techniques, scaling to a large number of qubits[12]. Superconducting qubits coupled to microwave resonators is the road cho-

sen by Google or IBM [3] to create their quantum computers.

Microwave resonators are devices that come into resonance at specific frequencies; that is, the amplitude of the field inside the resonator being probe externally is maximized at certain resonant frequencies. Many experiments have been performed in which a superconducting two-level system, playing the role of a qubit, is coupled to an on-chip cavity consisting of a superconducting transmission line resonator [13, 14, 6]. Superconducting resonators have recently been used in a multitude of scientific applications such as amplifiers, magnetic field resonators, optical detectors for UV or x-rays, and especially in quantum computing applications [15, 16, 17, 18]. These systems are ideal for control, readout, or for coupling pairs of qubits to each other using it as a quantum bus [19, 3, 15].

Circuit quantum electrodynamics (QED) architecture, in which a superconducting qubit is coupled strongly to a photon bound to a superconducting resonator, is used nowadays as a platform for performing quantum optics experiments [20] and for quantum information processing with superconducting circuits [15, 18]. In that sense, the quality factor (Q) of the resonator is essential in order to maximize the lifetime of a single photon (with frequency f) defined by $\tau = Q/2f$ [16]. With the resonator made of a superconducing material, its internal quality factor (Q_{int}) is maximized to neglect internal losses and enhance photon lifetime. Adding input and output capacitors, the resonator is externally loaded to enable fast measurements [15, 18].

Experiments have shown that coplanar waveguides (CPW) are a very suitable platform to interface resonators and superconducing qubits coherently [16, 15, 18, 14, 17]. CPW geometry consists of a center strip and lateral ground planes that can be designed to operate around several GHz (normally 5-15 GHz), being relatively insensitive to kinetic inductance and dominated by geometrically distributed inductance [18]. In comparison to other distributed element resonators, such as microstrips, the impedance can be controlled by lateral sizes from millimeters down to micrometers, with lateral dimensions essential to realize resonators with extremely large vacuum fields [21], and consequently for realizing strong coupling between photons and qubits [15]. In terms of fabrication, lithography process is used in order to pattern millimeter or micrometer structures [22, 23]. Many experiments have used silicon (Si) or sapphire (Al_2O_3) as dielectric substrates, with aluminum (Al) or Niobium (Nb) as superconducting materials using metal evaporation methods [15, 17, 18].

Recently, several of important advances have been made in the development of quantum computer prototypes. IBM already has several quantum computers on the cloud, having launched the last one of 53 qubits recently[24]. Moreover, a few months ago, Google, using a 53-qubit device, in collaboration with NASA, released a paper that defended "the alleged quantum supremacy"[25]. Many research groups are focusing on this field to lead the next technological revolution of the next decades. Nevertheless, there are still several questions to be solved, such as if these computers will be able to speed advancements in areas like chemistry or drug development, financial modeling, and even climate forecasting. These questions will not be answered in this project, but it is expected that they can be answered in the coming years. This project is based on creating superconducting circuits, in particular superconducting CPW resonators, for coherent qubit-photon operations that will give us information about the interactions and their behavior.

1.2 Methodologies

Dr. Gemma Rius from the IMB-CNM-CSIC (Institute of Microelectronics of Barcelona) and Dr. Pol Forn-Diaz from IFAE (The Institute for High Energy Physics) have led previous works on fabricating thin-film superconducting circuits compatible with quantum computing applications. This project tries to aim for the consolidation and validation of the fabrication and design methods for resonators. IFAE has supported the simulations within this project and IMB-CNM has supported the device fabrication.

Several programs have been used:

- Sonnet software [26] for the design and simulation of the microwave circuit.
- Glade software to implement the designs, making them compatible with the programs used in the cleanroom at IMB-CNM.
- Kloe 650 software for the photolithography process.
- Wolfram Mathematica to calculate several parameters accurately.

1.3 Project structure

An introductory chapter 1 is divided into three sections: a historical introduction of the topic, the methodologies followed and the project structure. In chapter 2, microwave theory in transmission lines is introduced, with a description of the resonator model implemented. In chapter 3, the resonator design is presented detailing parameters and explaining the influence of materials and dimensions. Section 4 provides the fabrication process, including the equipment used and the results obtained. Finally, the conclusion of the work is presented, explaining what has finally been achieved, and its possible outcomes.

At the end of the work, five annexes are included. In Annex A, the transmission line theory is presented. In Annex B, an extension of test simulations is added. Annex C provides a complete explanation of the lithographic process, and in Annex D, the equipment used and some methodology issues found. Furthermore, in Annex E, a complete introduction about state of the art is presented. Additional annexes, about acronyms and bibliography, are also included.

Chapter 2

Transmission line theory for microwave resonators

In this chapter, the transmission line (TL) theory is discussed for the particular case of an open-circuited $\lambda/2$ resonator. Due to the page limit in the thesis, Annex A has been added explaining the origin of some expressions that will appear along this part.

2.1 Microwave theory for transmission lines

In this section, a general model of TL is explained, making special emphasis on general expressions to create resonator circuits.

Normally, a TL is represented as a two-wire line, since transmission lines (for transverse electromagnetic [TEM] wave propagation) have at least two conductors. In figure 2.1 voltage $V(z,t)$ and current $I(z,t)$ are defined within an equivalent circuit model of length Δz of a TL.

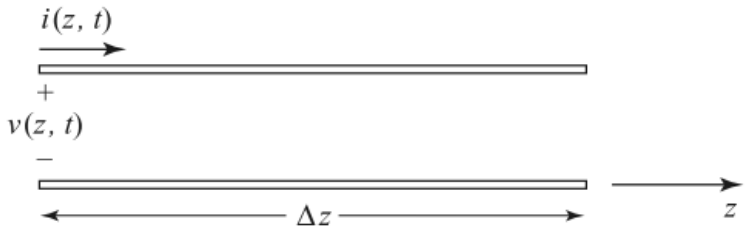

Figure 2.1: General circuit for a two-wire transimission line [27]

The equations of motion $V(z,t)$ and $I(z,t)$ in this TL take the following form (see Annex A for details):

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0, \tag{2.1}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0. \tag{2.2}$$

where γ is the complex propagation constant that is dependent on frequency ω [27].

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}. \tag{2.3}$$

γ depends on attenuation α and the phase constant β (depends on frequency), and on intrinsic parameters per unit length: resistance R, conductance G, inductance L

and capacitance C. Thus, after resolving 2.1 - 2.2 equations, and considering a lossless transmission line and also lossless terminations, the voltages and currents can be rewritten as:

$$V(z) = V_0[e^{-j\beta z} + \Gamma e^{j\beta z}], \tag{2.4}$$

$$I(z) = \frac{V_0}{Z_0}[e^{-j\beta z} - \Gamma e^{j\beta z}]. \tag{2.5}$$

Γ is the reflexion coefficient (see Annex A). The attenuation α can be rewritten as a sum of four different components:

$$\alpha = \alpha_C + \alpha_D + \alpha_G + \alpha_R. \tag{2.6}$$

α_C corresponds to loss due to metal conductivity, α_D to dielectric loss tangent, α_G due to conductivity loss of the dielectric and α_R due to radiation loss. In chapter 3 discusses how all attenuations have been neglected by choosing the right geometries and materials.

Applying Ohm's law the characteristic impedance Z_0 can be obtained.

$$\frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} = Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{\frac{L}{C}}, \tag{2.7}$$

which depends upon the material used. The input impedance Z_{in} is the impedance seen by a power source when connected to the TL, and determines how much power in the signal is reflected from the circuit.

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)}. \tag{2.8}$$

Z_L is an arbitrary load impedance, and l the length of the TL. In next section, R and G are neglected since we consider a lossless line. Further information is presented in Annex A.

2.2 Resonator model

TL resonators are devices which can be understood as systems that oscillate electromagnetically with greater amplitude at specific frequencies (called resonant frequencies). Nowadays, resonators are used for many purposes but mainly for electronic applications such as filters, oscillators, etc. Resonators can also be designed for applications in superconducting qubit circuits, such as control, readout, or couple individual qubits to each other as a quantum bus [18, 16].

In next subsections, the equivalent circuit model for microwave resonators; the TL resonator as an open-circuited $\lambda/2$ line; and the quality factor parameters are discussed.

2.2.1 Parallel resonant circuit

Near resonance, resonators can be presented as equivalent of series or parallel RLC components [27]. A parallel circuit is shown in figure 2.2.

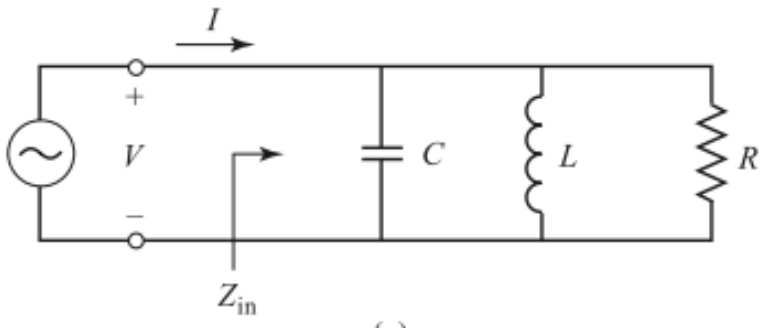

Figure 2.2: Parallel RLC circuit model for MW resonators [27]

The input impedance Z_{in} can be written as:

$$Z_{in} = \frac{1}{\frac{1}{R} + \frac{1}{j\omega L} + j\omega C}. \tag{2.9}$$

Applying the Ohm's law, the input power P_{in} [27] is given by:

$$P_{in} = \frac{1}{2} V I^* = \frac{1}{2}|V|^2 (\frac{1}{R} + \frac{j}{\omega L} - j\omega C). \tag{2.10}$$

The power losses P_{loss}, due to dissipation by the resistor is given by:

$$P_{loss} = \frac{1}{2}\frac{|V|^2}{R}. \tag{2.11}$$

W_m is the magnetic energy related to the inductance L and W_e is the electric energy related to the capacitance C. Their expressions are given by:

$$W_m = \frac{1}{4}|V|^2 \frac{1}{\omega^2 L}, \tag{2.12}$$

$$W_e = \frac{1}{4}|V|^2 \frac{1}{\omega^2 L}. \tag{2.13}$$

Rewriting the power delivered to the resonator [27], we get

$$P_{in} = P_{loss} + 2j\omega(W_m - W_e). \tag{2.14}$$

The resonant frequency ($\omega_0 = 2\pi f_0$) happens when $W_e = W_m$,

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{2.15}$$

2.2.2 Transmission line resonators: Open-Circuited $\lambda/2$ line

In order to achieve resonators with high quality factors, the design of the resonator is chosen as an open-circuited $\lambda/2$ line at both sides (λ is the wavelength). Such a device behaves as a parallel resonant circuit with length $l = n\lambda/2$ (see figure 2.3) with n the resonant mode number (n > 0). Thus, assuming that for the fundamental mode ($l = \lambda/2$) $\omega = \omega_0$, and letting $\omega = \omega_0 + \Delta\omega$ [27],

$$\beta l = \pi + \frac{\pi\Delta\omega}{\omega_0}. \tag{2.16}$$

Rewriting Z_{in} as

$$Z_{in} = Z_0 \frac{1 + \tan(\beta l)\tanh(\alpha l)}{\tanh(\alpha l) + j\tan(\beta l)}, \tag{2.17}$$

and approximating

$$\tan(\beta l) = \tan(\frac{\pi\Delta\omega}{\omega}) \approx \frac{\pi\Delta\omega}{\omega_0}, \tag{2.18}$$

$$\tanh(\alpha l) = \alpha l, \tag{2.19}$$

The input impedance can be rewritten as:

$$Z_{in} = \frac{Z_0}{\alpha l + j\frac{\pi\Delta\omega}{\omega_0}}. \tag{2.20}$$

In figure 2.3, a representation of the four first resonant frequencies along the TL is shown.

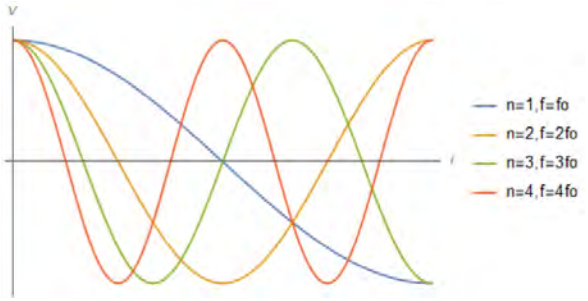

Figure 2.3: Voltage distributions over the resonator length ($l = n\lambda/2$), for the first four harmonics.

2.2.3 Quality factors of the resonator

One of the most important parameters, in the resonator, is the quality factor (Q), which gives us information between stored energy and dissipated energy, and is related to the sharpness of the resonant frequency. $W_e = W_m$ is fulfilled at $\omega = \omega_0$ [27], so internal quality factor Q_{int}:

$$Q_{int} = \omega \frac{W_e + W_m}{P_{loss}} = \omega_0 \frac{2W_m}{P_{loss}} = \frac{R}{\omega_0 L} = \omega_0 RC. \tag{2.21}$$

Equation 3.14 says that the quality factor is directly proportional to the intrinsic parallel resistance R, and C, and inversely proportional to the product of the resonant frequency ω_0 and L. Thus, the higher the resistance, more current will pass without ohmic losses providing a high quality factor. In equation 3.14 did not consider loading effects, caused by external circuitry. Considering the parallel resonant circuit model of subsection 2.2.1, the correct expression, when coupled to a power source, is the parallel sum of two quality factors, one internal Q_{int} and the other external (loaded) Q_{ext} [15, 28]:

$$\frac{1}{Q_{total}} = \frac{1}{Q_{int}} + \frac{1}{Q_{ext}} \tag{2.22}$$

Chapter 3 discusses how the external quality factor might take over the total quality factor, putting special emphasis on increasing the internal quality factor by using the superconducting materials and geometries.

Chapter 3

Design of coplanar waveguide resonators

The previous chapters were introducing the general theory of transmission lines and resonators. The proposal is to design superconducting resonators with high-quality factors for quantum computing applications. In this part, the resonator geometry is presented together with the materials needed. The equivalent circuit model (previously introduced in chapter 2) will be followed. Finally, we will show the circuit and the simulation results.

3.1 Materials and geometry choice

The main purpose is working with a thin film superconductor material. Special attention has been paid in the selection of materials (Al and Si) and geometry, being coplanar waveguide (CPW) type [15, 16, 18].

3.1.1 Substrate

The substrate is **Silicon (intrinsic)** (Si). Previous works [15, 17, 18] have shown the good properties of this material when combined with superconducting resonators, in addition to the widespread use in the field of electronics [29]. Since superconductors are mostly lossless, the loss tangent of the Si dielectric layer controls the overall loss of the circuit. A small value is chosen to simplify the device analysis and in this way concentrate only on external system loss coming from the external circuitry [30]. In table 3.1 the Si parameters used are presented, with ϵ_0 and ϵ_{eff} being the relative and effective permitivity, respectively.

Substrate material	**Thickness**	ϵ_r	ϵ_{eff}	**Conductivity**	**Loss tangent**
Silicon (intrinsic)	500 μm	11.9	6.38	0 (S/m)	$3 \cdot 10^{-6}$

Table 3.1: Important non-doped silicon properties as a substrate material for the CPW resonator design.

3.1.2 Metal layer

The metal layer is **Aluminum** (Al). Previous works have shown this material as a good superconductor for building quantum computing applications, specially supercon-

ducting resonators [19, 15, 17, 18]. *Al* is a well-known chemical element in microfabrication at IMB-CNM-CSIC, having, a convenient boiling point for reliable metallization over silicon wafers. Its critical temperature (T_c) (temperature which at the metal becomes a superconductor, $T_C(Al) \approx 1.2K$) can be easily reached in a cryogenic refrigerator. In the superconducting state, the material ceases to exhibit energy dissipation, having a null resistance to the passage of current [31]. In Table 3.2 the general aluminum properties are presented.

Substrate material	**Thickness**	T_c	**Boiling point**	**Conductivity**
Aluminum	100 nm	1.2 K	2753,15 K	∞ (S/m)

Table 3.2: Aluminum properties, as a metal layer material, for the resonator design.

3.1.3 Coplanar waveguide geometry

CPW geometry is used in many applications such as amplifiers, active combiners, mixers, etc [32, 15]. CPW is a planar transmission line, characterized by one center conductor strip W in the middle of two ground (GND) planes on top of the substrate, separated by a distance S (see figure 3.1).

The properties of CPW are well-known. Some advantages of this geometry are: great isolation, low dispersion, low ground inductance for shunt elements (compared, for instance, to microstrip applications), simple realization due to etching in only one side and cheaper and faster than other geometries [32, 33, 34]. [1].

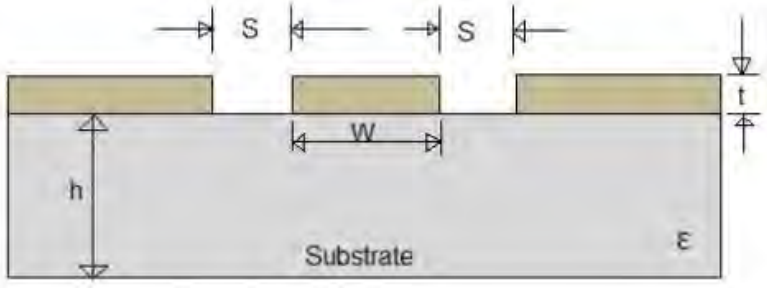

Figure 3.1: Cross-sectional view of coplanar waveguide geometry, with different dimensional parameters S, W, h and t [34]

In figure 3.1, the parameters needed to define the CPW throughout the structure, are shown. h and t are the dielectric and metal thickness, respectively. A characteristic impedance of $Z_0 \approx 50\Omega$ is achieved with the values presented in Table 3.3[2]. In CPW geometry, the width of the ground planes needs to be large enough to achieve good ground isolation (usually the width of GND planes should be larger than $\lambda/10$) [32]. The parameters, shown in Table 3.3, yield a characteristic impedance $Z_0 = 50\Omega$, which is necessary to interface to conventional microwave components and instruments in the GHz range.

[1] In Annex B CPWG geometry grounded via hole is presented
[2] better explanation is given in section 3.2

W	S	t	h
10 μm	6 μm	100 nm	500 μm

Table 3.3: Parameters for the CPW geometry used to design the superconducting resonator.

External signals can propagate down the TL until the arrive at the resonator, which is intersected by two gaps in the TL, defining in this way the input/output coupling capacitors. In figure 3.2 a simple top view of CPW geometry is shown. Capacitors have been designed on both sides of the transmission line (gap capacitors) to modulate the quality factor of the resonator.

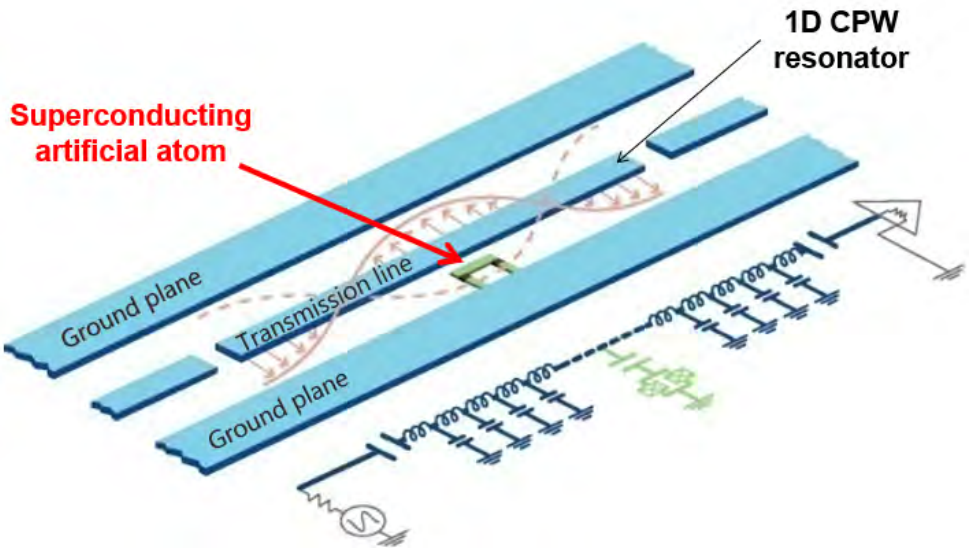

Figure 3.2: Top view of coplanar waveguide geometry coupled to a qubit [14].

3.1.4 Capacitor geometry

Capacitors have been designed for two different geometries, finger capacitors ((a) figure 3.3) and gap capacitors ((b) figure 3.3). Different dimensions, of each capacitor type, have been designed to study the change in the coupling capacitance.

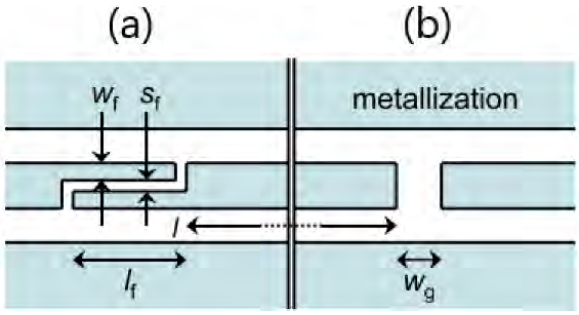

Figure 3.3: Top view of different capacitors used in the CPW resonator. (a) finger 1+1 capacitor (b) gap capacitor [15]

In simulations have been simulated finger 1+1, 2+2 and 3+3 capacitors with parameters $w_f = 4\mu m$, $s_f = 4\mu m$ and $l_f = 116\mu m$, and gap capacitors of w_g =10, 30, 50 μm.

3.2 Equivalent circuit

The resonator is usually coupled to an external circuit, with input and output load resistance R_L and coupling capacitance C_k, which modulates the resonator quality factor (Q_{ext}) (equation 2.22).

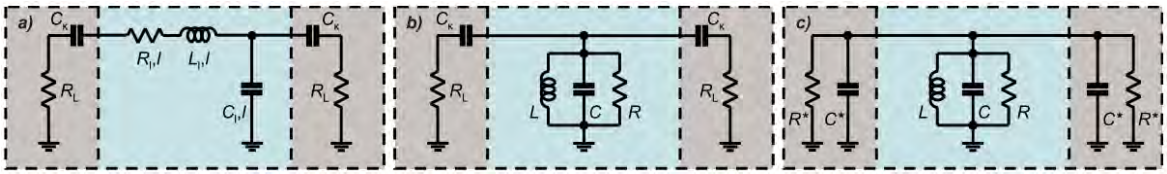

Figure 3.4: Equivalent circuit models for the CPW resonator, extracted from [15]. a) Distributed element representation of symmetrically coupled TL resonator, b) Resonator represented as a parallel RLC circuit, c) Norton equivalency of symmetrically coupled parallel RLC resonator.

Following from ref. [15], in figure 3.4, three different equivalent circuits are shown. L_l ,R_l and C_l denote inductance, resistance and capacitance per unit length. The resonator is modeled as a pair of input and output capacitors and resistances connected to ground, with the TL resonator driven near its resonance, represented by a RLC parallel circuit (b. figure 3.4). Norton equivalency is applied (c. figure 3.4) to simplify quality factor calculations. The resonance frequency of the fundamental mode is given by:

$$f_0 = \frac{c}{2l\sqrt{\epsilon_{eff}}} = \frac{c}{\lambda\sqrt{\epsilon_{eff}}}, \tag{3.1}$$

c is the light speed and the effective permitivity ϵ_{eff} is a function of the resonator geometry (equation 3.2). Resonant frequency f_0 depends on the length l of TL. Different resonators are designed from 6.7 GHz to 6.9 GHz, with the length between l = 8.863 mm and l = 8.606 mm, respectively.

Previously mentioned in chapter 2, all attenuations are neglected, α_C (metal conductivity losses) due to superconductivity, α_R (radiation losses) due to CPW geometry, and α_D (dielectric loss tangent) and α_G (dielectric conductivity losses) because of cooling the circuit in the cryogenic refrigerator when measured [30, 23, 35]. The phase velocity v_{ph} is defined as:

$$v_{ph} = \frac{c}{\sqrt{\epsilon_{eff}}} = \frac{1}{\sqrt{L_l C_l}}. \tag{3.2}$$

where

$$L_l = \frac{\mu_0}{4}\frac{K(k_0^{'})}{K(k_0)}. \tag{3.3}$$

$$C_l = 4\epsilon_0\epsilon_{eff}\frac{K(k_0)}{K(k_0^{'})}. \tag{3.4}$$

K denotes the complete elliptic integral of the first kind with geometric arguments (Table 3.3):

$$k_0 = \frac{W}{W+2S}. \tag{3.5}$$

$$k_0^{'} = \sqrt{1-k_0^2}. \tag{3.6}$$

$L_l = L_l^m + L_l^k$ depends on the kinetic inductance L_l^k and on magnetic inductance L_l^m. L_l^k is related to the inertia of moving Cooper pairs[3], to London penetration depth [4] and is dependent on temperature . L_l^m is independent on temperature [15, 36]. Non-magnetic materials are used i.e. effective permeability $\mu_{eff} = 1$, and L_l, C_l and ϵ_{eff} depend on geometry [15]. The resonator impedance is defined as:

$$Z_0 = \sqrt{\frac{L_l}{C_l}}. \tag{3.7}$$

$Z_0 = 50\ \Omega$ needs to be satisfied along the line. The equivalent RLC model of the TL line requires the following parameter relations:

$$L_n = \frac{2L_l l}{n^2\pi^2}, \tag{3.8}$$

$$C = \frac{C_l}{2}, \tag{3.9}$$

$$R = \frac{Z_0}{\alpha l}. \tag{3.10}$$

Inductance L_n , capacitance C and resistance R depend on the length l. L_n depends on the resonant mode n ($n > 0$) and parallel resistance R is inversely dependent on attenuation.

To see how coupling capacitance C_k affects the shift in the resonant frequencies, Norton equivalency is applied (see c. figure 3.4).

$$R^* = \frac{1 + w_n^2 C_k^2 R_L^2}{w_n^2 C_k^2 R_L}. \tag{3.11}$$

$$C^* = \frac{C_k}{1 + w_n^2 C_k^2 R_L^2}. \tag{3.12}$$

Where $\omega_n = 2n\pi f_0$ for $n > 0$, R_L is the load impedance and C_k the coupled capacitance. The smaller the capacitance C_k the greater the load parallel impedance R^*. The shift in the resonant frequency ω_n^* [15] is given by:

$$\omega_n^* = \frac{1}{\sqrt{L_n(C+2C^*)}}. \tag{3.13}$$

Symmetric capacitors are designed at both sides. Thus, considering $\omega_n \simeq \omega_n^*$, the total quality factor (Q_{total}) is the parallel sum of the external (Q_{ext} , due to coupling) and internal (Q_{int} , intrinsic TL resonator) (see equation 2.22).

$$Q_{int} = \omega_n RC = \frac{n\pi}{2\alpha l}. \tag{3.14}$$

[3] Cooper pairs: Pair of electrons created because of superconductivity [31].

[4] Penetration depth: Penetration of a magnetic field into a superconductor [31]

$$Q_{ext} = \frac{\omega_n R^* C}{2} \tag{3.15}$$

Equations 3.14 and 3.15 are satisfied only near resonance [15]. If $Q_{int} \rightarrow \infty$, Q_{total} is influenced only by Q_{ext}. Modulating C_k the desired quality factor is obtained, fulfilling $Q_{total} \simeq Q_{ext}$. In Table 3.4 numerical values, obtained for the fundamental mode of $f = 6.9$ GHz, are presented.

L_l	C_l	v_{ph}	Z_0
$4.236 \cdot 10^{-7}\ H/m$	$1.694 \cdot 10^{-10}\ F/m$	$1.180 \cdot 10^{8}\ m/s$	$50.006\ \Omega$

Table 3.4: Numerical values of important parameters calculated for designing the CPW resonator.

3.3 Simulation results

Simulations are performed using Sonnet Software. This section is divided into two parts, a first design, which is later, fabricated in the cleanroom (see chapter 4), and a second optimized design. In both, the same conditions are applied according to Sonnet documentation [26]. This software simulates circuits in a six-face box, allowing to change the top and bottom covers. To avoid box resonances, no metal covers are used, so Free-space option was applied. For CPW geometry, negative ports are added for ground planes (-1 and -2 ports setting the same potential), and the positive ones for measuring the response. All ports are connected to a load impedance $Z_L = 50\Omega$. Four different layers are created: 1000 μm of air, at the top and at the bottom, and two internal ones: 500 μm of Si and above 100 nm of Al (both lossless) (see figure 3.5, material values extracted from Tables 3.1 and 3.2).

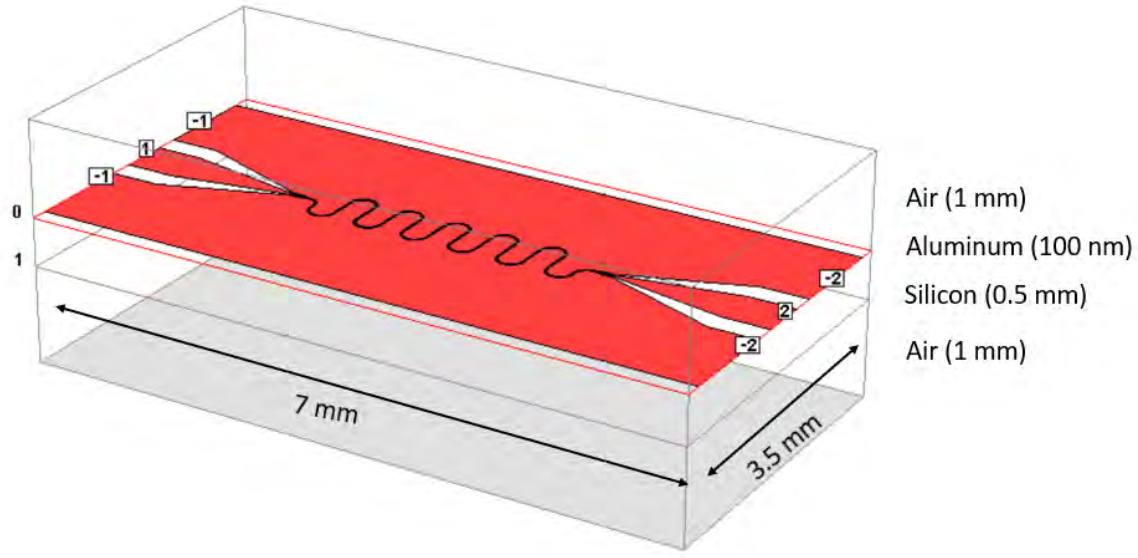

Figure 3.5: Representation of the superconducting coplanar waveguide resonator (first design) by Sonnet software. 3D view. Capture taken from Sonnet software.

Due to lack of size restrictions, the first design is 7000 μm x 3500 μm. Nevertheless, in second design the size was optimized, in time simulations, with a chip size of 2800 μm x 2600 μm.

3.3.1 First design

In figure 3.6, the circuit is divided into three different parts, two symmetrical capacitors (green lines fig. 3.6), two symmetrical connectors (yellow lines fig. 3.6) and the meander (blue line fig. 3.6). Connectors and capacitors determine Q_{ext} and the meander determines Q_{int}. The rectilinear transmission line is transformed into a meander, preserving the conditions with separations between each meander of 238 μm . The main reason why capacitors and connectors have different width W/S ratio respect to TL, is the conservation of the characteristic impedance Z_0 along the resonator. Moreover, connectors end in $W = 500\mu m$ and $S = 244\mu m$ because of size limitations when soldering them in experimental measurements [37].

The resonator spectrum can be measured experimentally with the Vector Network Analyzer (VNA) [16, 18]. The resonant frequencies might be typically understood as Lorentzian peaks [15]. The sharpness of the peaks characterizes the quality factor of the resonator, as $Q_{total} = f_0/\delta f$, being δf the Full Width at Half Maximum (FWHM) located at $-3dB$.

Resonant peaks are shown in figure 3.7, by using the graphical interface in Sonnet. In software, the scattering parameters are simulated using the Scattering matrices (shown in Annex A). S_{21} is the transmission parameter that gives information about the power delivered from port 1 to port 2. In figure 3.7 the S_{21} of the CPW resonator is presented, for the two first resonant frequencies, being symmetrically coupled by two finger 2+2 capacitors. The fundamental mode is located at 6.9 GHz, being the power delivered maximum $S_{21}(f_0) \simeq 0dB$, and the total quality factor $Q_{total} = 552$.

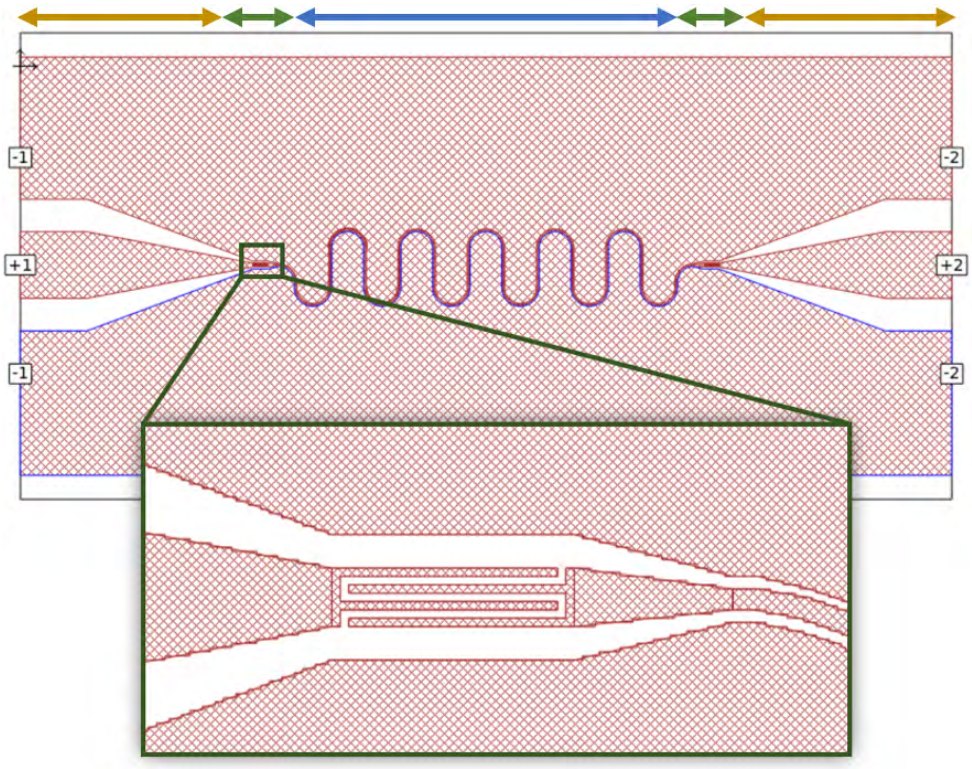

Figure 3.6: Geometric representation of the superconducting coplanar waveguide resonator (first design) by Sonnet software. 2D view. Magnification of a finger 2+2 capacitor. Capture taken from Sonnet software.

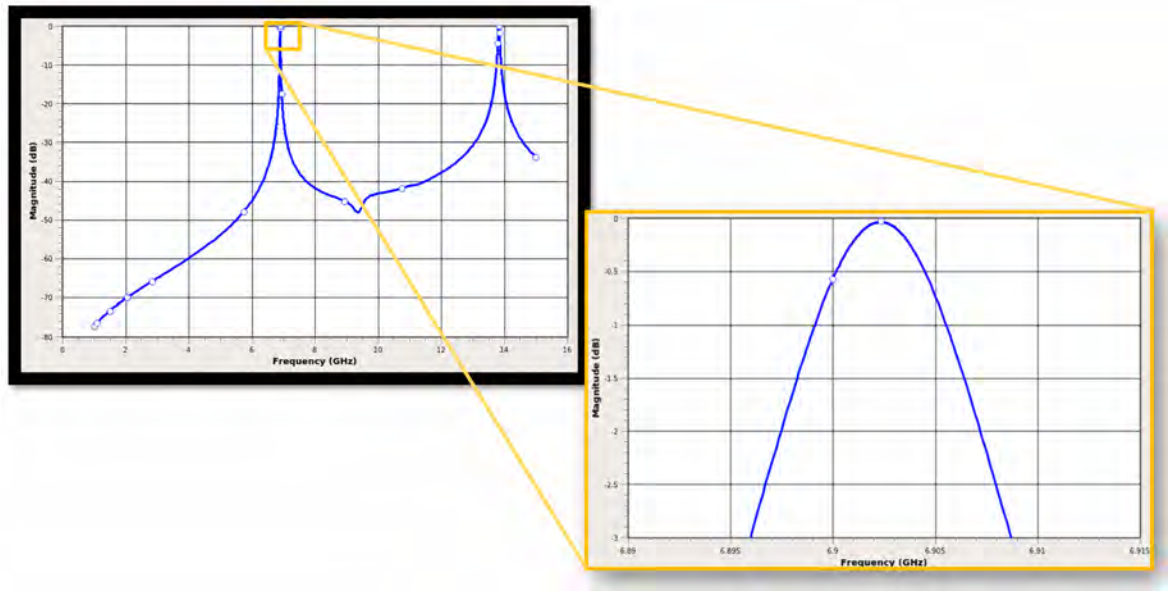

Figure 3.7: Representation of S_{21} parameter (in dB) for a CPW resonator (first design) with two symmetrical 2+2 finger capacitors. Simulation for a range of 0-16 GHz, and magnification of the fundamental mode frequency. Capture taken from Sonnet.

3.3.2 Optimized design

A second design is analyzed with size chip 2800 μm × 2600 μm (the circuit is optimized in size, in order to reduce time simulations). The meanders have been lengthened and the spacing between them is reduced to 70 μm (see figure 3.9). A study of different resonators, is given in figure 3.10, presenting how coupling capacitance affects to the response. Six resonators, with different symmetrically coupled capacitors are designed, at fundamental frequencies of 6.7 GHz.

Table 3.5 values shows, the greater the coupling capacitance, the smaller the total quality factor. Furthermore, increasing capacitance, transmission losses decrease, with $Q_{int} \approx 2.7 \cdot 10^5$. In figure 3.10 the transmission response of the C_k is plotted over the fundamental mode of each resonator. A shift in the resonant frequency is observed due to coupling capacitance, this is in agreement with equation 3.13 [15]. As C_k becomes greater, f_0 decreases.

ID	**Coupling**	$C_k(fF)$ (theory)	$f_0(GHz)$	Q_{total} (simul.)	$C_k(fF)$ (simul.)	$S_{21}(dB)$
A	3+3 finger	28.35	6.43	$2.26 \cdot 10^2$	27.01	-0.007
B	2+2 finger	16.64	6.54	$6.43 \cdot 10^2$	15.85	-0.017
C	1+1 finger	5.46	6.66	$5.85 \cdot 10^3$	5.19	-0.133
D	10 μm gap	0.49	6.775	$1.96 \cdot 10^5$	0.65	-1.167
E	30 μm gap	0.34	6.777	$2.29 \cdot 10^5$	0.43	-4.849
E	50 μm gap	0.27	6.778	$2.42 \cdot 10^5$	0.38	-10.682

Table 3.5: CPW resonator parameters for the different simulated coupling capacitances (optimized design).

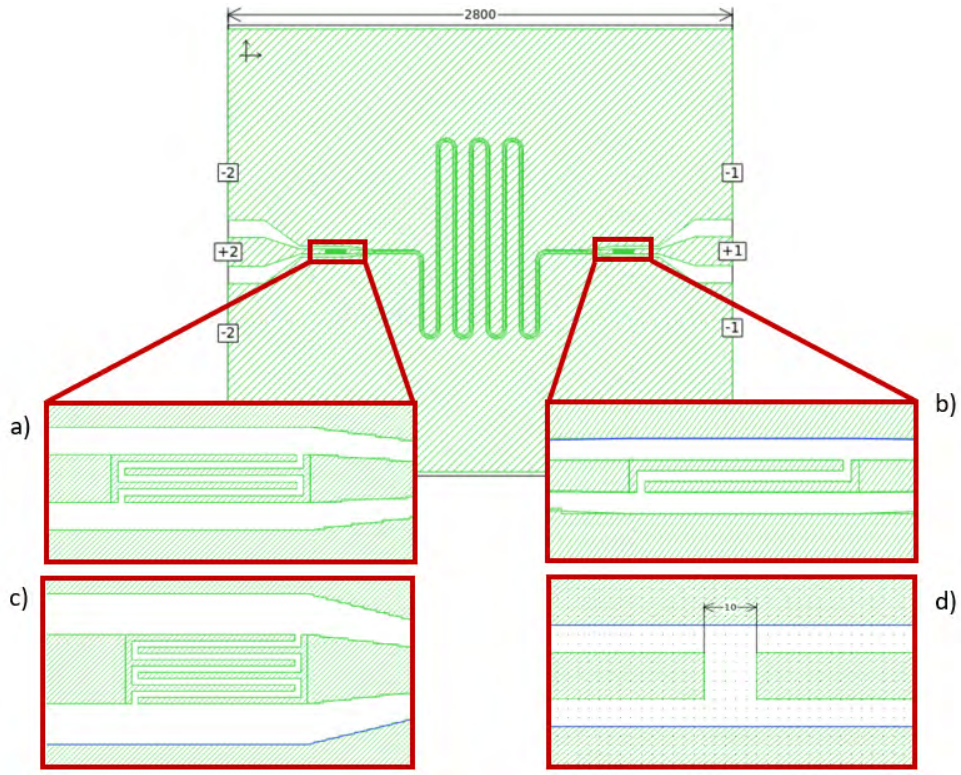

Figure 3.8: Geometric representation of the superconducting coplanar waveguide resonator (optimized design) by Sonnet software. 2D view. Magnification of a (a) finger 2+2 capacitor, (b) finger 1+1 capacitor, (c) finger 3+3 capacitor, (d) gap 10 μm. Capture taken from Sonnet software.

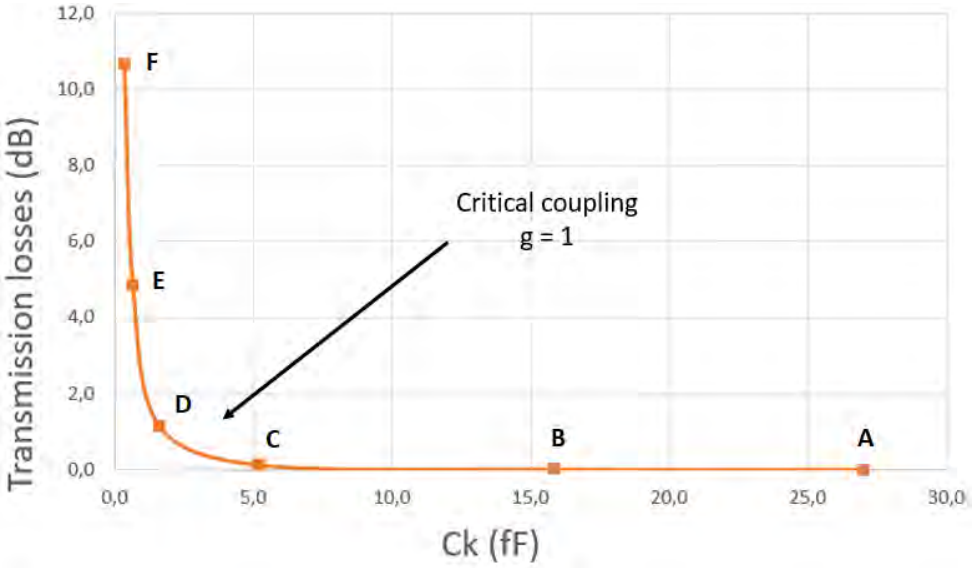

Figure 3.9: Distribution of transmission losses (in dB) over the coupling capacitance C_k (in fF) for a six CPW resonators with two symmetrical capacitors (values represented in table 3.5). Shown fundamental modes.

The coupling capacitance continuously decreases from device A to E, and it also decreases in terms of transmission losses ($S_{21} \rightarrow 0$(dB)). This dependence is shown in

equation 3.16, extracted from [38].

$$S_{21} = \frac{1}{R_c/R} \frac{1}{1 + j2Q_{total}(\omega - \omega_0)/\omega_0} \tag{3.16}$$

where $R_c = 1/(\omega C_k)^2/(2Z_0)$. Figure 3.9 shows two well-differentiated cases using the critical coupling parameter ($g = Q_{int}/Q_{ext}$), for $Q_{int} \approx 2.7 \cdot 10^5$. The first regime (undercoupled regime $Q_{ext} >> Q_{int}$) is determined because internal losses dominate over external losses, which is the case of the D-F gap capacitors. The second regime (overcoupled regime $Q_{ext} << Q_{int}$), external losses dominate over the internal ones (fulfilling $Q_{ext} = \frac{C}{2\omega_n R_L C_k^2}$), being this region determined by finger capacitors A-C.

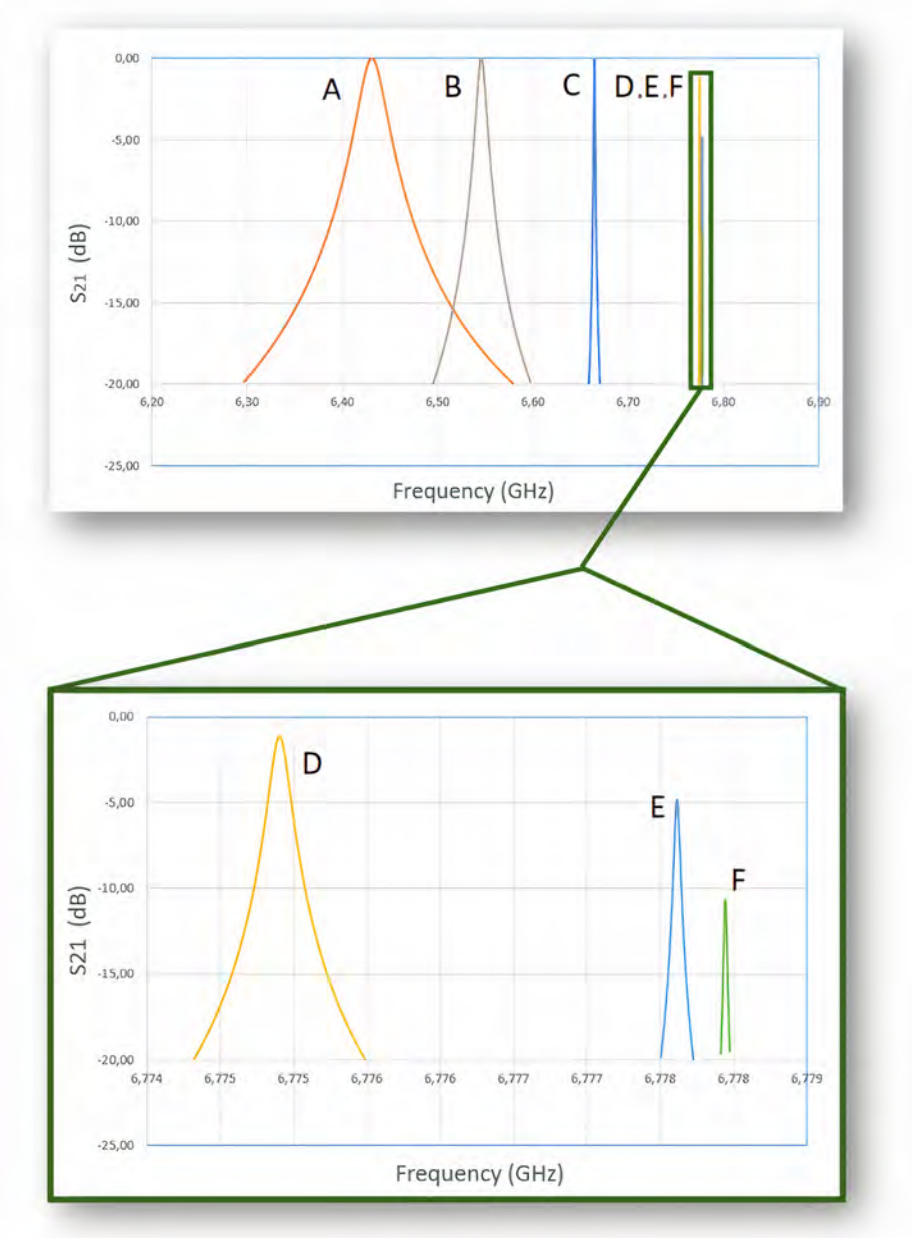

Figure 3.10: Fundamental mode distribution of S_{21} parameter (in dB) for six different CPW resonators (optimized design), with two symmetrical capacitors. A-C finger capacitors (image above), and D-F gap capacitors (image below) (values extracted from Table 3.5).

The spectrum of the first three harmonic modes for a CPW resonator B ($\omega_n = n\omega_0$ with n=1,2,3), is observed in figure 3.11. The S_{21} (blue lines fig. 3.11) and S_{11} (red lines fig. 3.11) parameters are represented for an overcoupled resonator B. S_{11} is the power reflected by port 1. When reflection is minimum, the transmission is maximum, fulfilling the resonant frequency definition [39]. Table 3.6 values correspond to results of figure 3.11. These values are in good agreement with equation $Q_{ext} = \frac{C}{2\omega_n R_L C_k^2}$, exhibiting a decrease in the quality factor with harmonic number. In terms of coupling qubits with superconducting resonators, the fundamental mode always presents better quality factor compared to the other harmonics. Since the resonator is in an overcoupled regime ($Q_{ext} << Q_{int}$), increasing the resonant frequency, Q_{ext} displays a decrease, having an influence on Q_{total}.

Harmonic mode	$f_0(GHz)$	Q_{total}
$\mathbf{1}^{st}$ mode	6.54	643
$\mathbf{2}^{nd}$ mode	13.08	317
$\mathbf{3}^{rd}$ mode	19.62	190

Table 3.6: Simulated parameters for the first three harmonics, in the optimized resonator design.

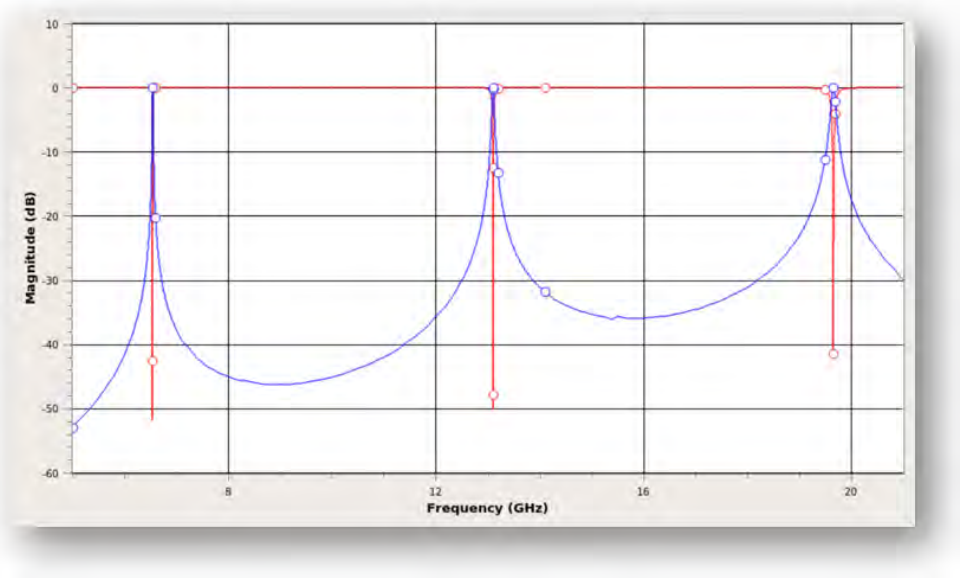

Figure 3.11: S_{21} parameter (in dB) over frequency (GHz). Distribution of the three first harmonics in a CPW resonator (optimized design). Overcoupled resonator B with two symmetrical finger 2+2 capacitors. Capture extracted from Sonnet.

As conclusion for this chapter, the results obtained in the simulation designs are in good agreement with previous articles [15, 16, 17, 18, 28], being able to state that the outcomes are consistent theoretically. Therefore, design process is validated.

Chapter 4

Fabrication of the CPW resonator

This chapter presents the fabrications developments for the first design, shown in section 3.3.1. The final goal would be to validate experimentally the results of the design and simulation of the CPW resonator. All the fabrication processes have been implemented in the cleanroom at the Microelectronics Institute of Barcelona (IMB-CNM).

In this chapter, the basic stages for fabricating superconducting CPW resonators are presented: the definition and description of the whole fabrication sequence, the design of the layout (with GLADE software), the setup and optimization of the lithography procedures (with KLOE 650 software), and the basic inspection of the outcomes obtained, before and after pattern transfer.

4.1 Introduction to fabrication

Some previous works [16, 15, 18, 28], have already shown some studies concerning the fabrication of superconducting CPW resonators. In all them, the strategy followed, to pattern millimeter or micrometer structures, is the optical lithography. The optical lithography, or also known as photolithography, is a microfabrication technique that uses photons in the UV frequency regime, around some hundreds of nm (375 nm in our case), to transfer a pattern to a photoresist [22]. This technique can pattern millimeter or micrometric shapes, and is based on light-sensitive resist, which is deposited on top of a thin film or the bulk of a wafer. As a rule, this process of light-exposure is made placing a mask on top of the substrate, which already has the patterns to be transferred to the thin film photoresist. However, in this work a particular implementation of photolithography is used. Precisely, a laser writer, installed in the cleanroom at IMB-CNM which is based on direct writing instead of a mask, and relies on specific beam steering, via KLOE 650 software [40]. Direct writing allows full design-flexibility which is very convenient when design has not been yet experimentally validated. The micrometer dimensions and resolution of the layout, for instance, finger electrodes require extremely clean conditions, that is why a cleanroom environment is needed. Similar requirement are imposed which concern the etching process [16, 22]. This process might be a chemical (wet) or/and physical (dry) process. For processing simplicity wet etching has been chosen in this work.

In figure 4.1 the whole fabrication sequence is shown. The chips consist in Aluminum 100 nm thick layer + Silicon 500 μm deposited by a E-beam evaporation. Then, the chip is cleaned and prepared for the photoresist deposition, by the so-called spin coating technique. After that, laser exposure and development of patterns are made,

by using the laser writer. Then, a wet etching process is applied, for the resist pattern transfer to the thin Al layer, and finally, the photoresist removal is done. Last two steps have been performed by the IMB-CNM Clean Room staff.

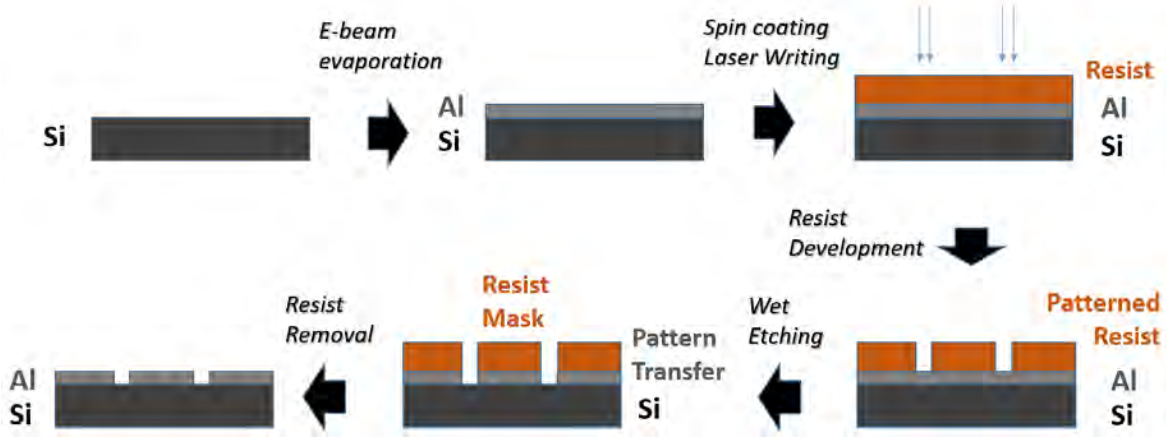

Figure 4.1: Processing sequence for the fabrication of the aluminum CPW resonators.

As laser writer is still an under development process at the IMB-CNM Clean Room, preliminary exposure tests have been done on silicon substrates (without Al). However, once suitable exposure conditions were obtained, chips of $Al + Si$ were tested. As for pattern transfer by etching, due to Al granularity [41], writing patterns on aluminum, and achieving good resolution, can become a critical process. In terms of dimensions (see chapter 3), there are structures which require resolutions of $1\mu m$, in the limit of the current laser writer capabilities, like finger capacitors, but other ones tens (meanders) or hundreds (connectors) micrometers.

4.2 Basic procedure

As previously discussed, the essential steps for CPW resonator are photolithography and an etching process. Ultraclean conditions are fundamental to avoid any dust, water, or whatever particle which might interfere with your fabrication procedure or alter the patterning results, as dust particles are typically in the micron scale, i.e. similar to our CPW structure dimensions. Additionally, the whole process, is done in a room with UV filters, to avoid unwanted photoresist exposure. There are some additional steps involved in the whole process, as follows:

- **Wafer cleaning**: remove contamination on the surface by a chemical treatment (use of acetone, ultrasounds, isopropanol, deionized water, and nitrogen gun).
- **Preparation for spin coating of the resist**: drive off any water or solvent particle of previous steps heating the wafer, using hot plates, and preparing the surface to increase adhesion of the photoresist, using hexamethyldisilizane (HMDS).
- **Photoresist deposition**: deposition of the S1805 positive photoresist in a liquid form. Step done with spin coater in vacuum conditions.
- **Soft bake**: improve photoresist adhesion and remove solvent rests, using hot plates.

- **Light exposure**: pattern with UV-light the desired layout, using laser writer.
- **Pattern transfer** : wet etching of the *Al* using the patterned photoresist as a mask.
- **Photoresist removal**: stripping of the resist in organic solvents.

Due to the size constraints, in this manuscript, a further description of the photolithographic process and the equipment used, is presented in Annexes C and D.

Regarding the laser exposure, some preparation steps need correctly steer the laser beam and obtain optimal definition of the different elements of the layout. Specifically, a proper choice of laser trajectories has to be done. To do that, the next steps were followed:

- Design the structure layout in **GLADE Software** and to export the files in ".gds" format.
- Import the ".gds" format in **KLOE design software**. Convert the different elements of the structures into trajectories (laser beam movement), and export it in a ".lwo" format.
- Import the ".lwo" format in the software called **KLOE Dilase 650**, defining the exposure parameters and launch the laser writing process.

Further details, of each step, is given in the next sections.

4.3 GLADE design

The goal is to obtain a real sample with the same dimensions as calculated and determined in Chapter 3. A replication of simulated structure is generated as a ".gds" file in GLADE Software, since it was not possible to export the file from Sonnet (see figure 3.1).

In figure 4.2, coloured polygonal elements are the structures that laser beam will write (connectors, in red, and the meander structures in yellow and green).

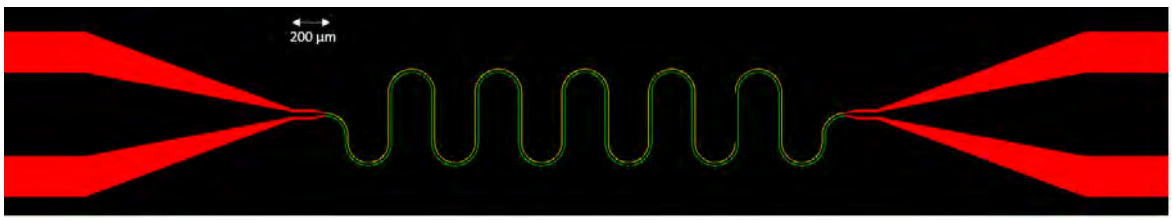

Figure 4.2: Resonator design made by GLADE software.

After that, ".gds" file is imported in KLOE design software.

4.4 Exposure strategy

As mentioned, the laser trajectories are generated in KLOE design software. KLOE is a direct writing laser, which designed to transfer patterns into films by a photopolymerization process. Some special technical principles of this technique include:

- Contour writing in X and Y axis, with a fixed focal position, thanks to the motion of the writing stage (flat chuck which holds the sample). But no curved trajectories can be done.
- Dynamic and continuous writing on planar substrates, having the possibility to write in positive or negative photoresists.
- Two laser spot sizes (10 μm or 1 μm), for which is possible to change velocity, modulation, focal length, and many other parameters to optimize the exposure results.

These writing capabilities are fundamental to define the laser trajectories and accurate pattern results. In KLOE software, filling trajectories might be automatically done, selecting the different structures. This mode has three different ways of transforming the polygons into trajectories:

- **Horizontal filling**: Horizontal lines used for the connectors.
- **Vertical filling**: Vertical lines used for the meanders.
- **Optimized filling**: Diagonal lines (this type of filling is not applied)

The choice of each filling was done depending on the size of polygons. For large structures, trajectories separation is 2 μm between each one. In figure 4.3 is presented the different filling modes applied to the connectors and meander.

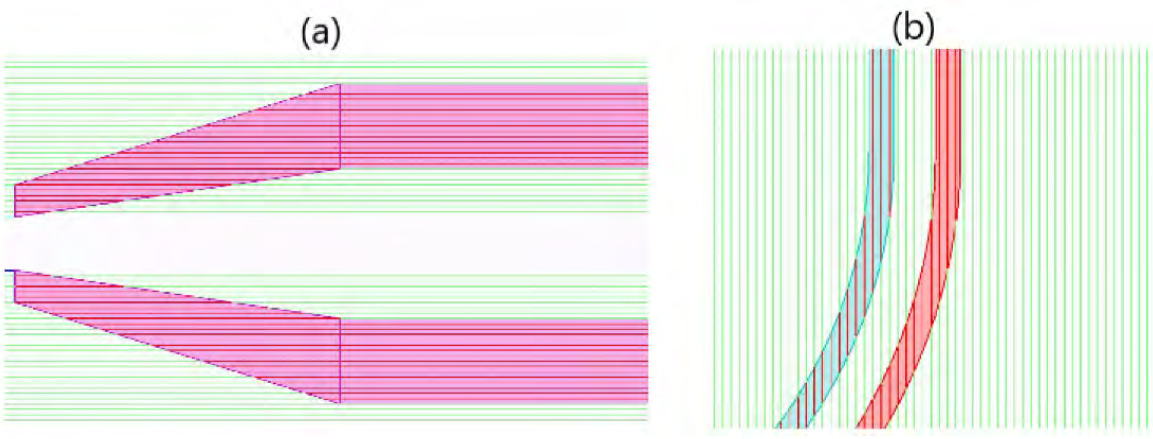

Figure 4.3: (a)Horizontal filling mode laser trajectories for connectors and (b) vertical filling mode for meanders, in a CPW resonator. Capture extracted from KLOE software. While laser beam follows all lines, the laser beam is ON only in the pink or red sections of the lines.

Concerning finger capacitors, due to the challenge in terms of feature size and resolution (smallest laser spot 1 μm, finger width and spacing in the order of few microns)

filling mode was not possible to implement it, so it was necessary the creation of specific line trajectories manually, to achieve enough resolution and feature accuracy. After many tests the best design solution, by combination of finely tuned grid lines, is presented in figure 4.4 for a 2+2 finger capacitor:

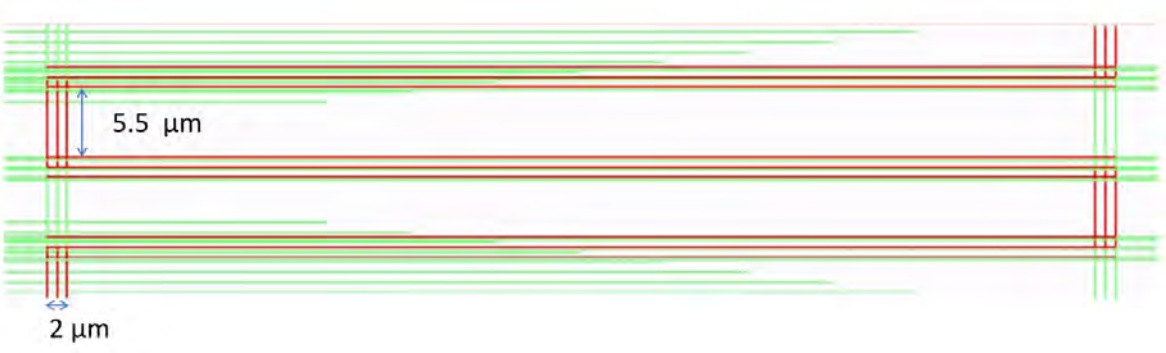

Figure 4.4: Laser trajectories for finger capacitors. Example of a finger 2+2. Capture taken from KLOE software.

In figure 4.4, red lines correspond to the time of laser is ON, conversely green lines when laser is OFF. The laser trajectories are separated 1 μm between each one, being a finger composed of three lines. Note also, the dedicated grid for definition of the joints. The dimensions showed should be preserved for $n+m$ finger capacitors. Once laser paths have been created, the files are exported in two separated ".lwo" files (fingers + full structure), to be imported in Kloe Dilase 650 software. All polygons consist in a finite number of parallel laser trajectories, being the effective pattern width of each one determined by the dose applied by the laser (spot size 1 μm) which is strongly correlated to the velocity and modulation. The suitable dose is the one that corresponds to a combination of the overlapped trajectories according to the Gaussian profile of the laser beam intensity, shown in figure 4.5.

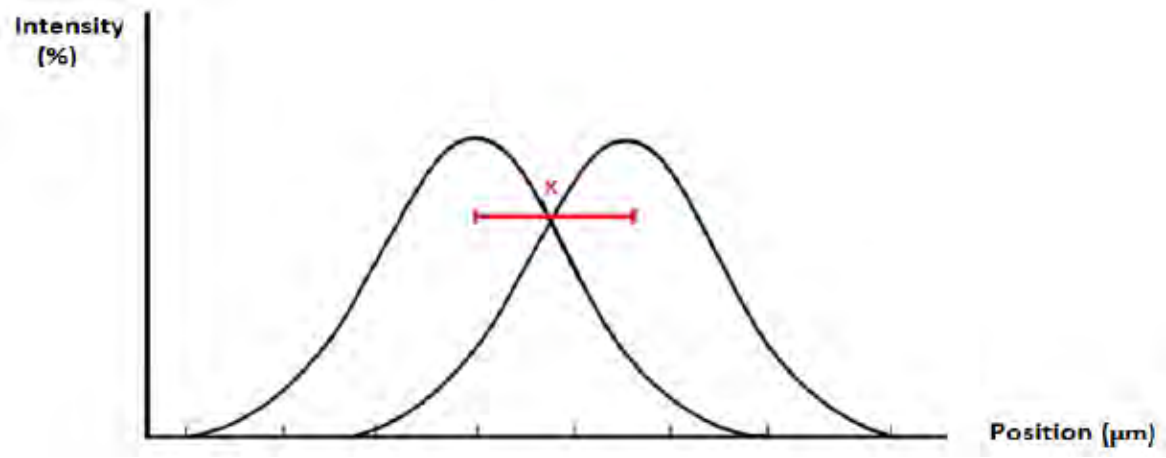

Figure 4.5: Gaussian distribution shape of two parallel laser beams [23].

The exposure parameters used, in Kloe Dilase 650, are:

- **Modulation**: modulation of the laser power, delivered to the photoresist, in %.
- **Writing velocity**: the stage movement during the exposure, in mm/s.
- **Return velocity**: the velocity of the motorized stage during the repositioning between 2 separate trajectories, in mm/s.
- **Focusing height**: the distance between the head of the laser and the wafer surface, in mm.

Additional information of the equipment is provided in Annex D. Many chips have been done in order to calibrate and adjust the different parameters. Table 4.1 shows the exposure values of filling mode, modulation and writing velocity for the S1805 positive photoresist. Focusing height and return velocity are common for any structure. As observed, the best values are different depending on size and resolution of the different elements. In the meander and connectors same modulation and writing velocity can be used. However, in finger capacitors different values are applied, also trajectories spacing differs. The writing velocity and modulation changes the control of the beam delivery, being very accurate the parameters depending on each structure.

Structure	Filling mode	Modulation	Writing vel.	Focusing height
Connectors	Auto: Horizontal	8%	1 mm/s	-2.157 mm
Meanders	Auto: Vertical	8%	1 mm/s	-2.157 mm
Finger capacitors	Manual	15%	2 mm/s	-2.157 mm

Table 4.1: Most suitable exposure conditions (KLOE 650 Dilase software) obtained for the different structures in the CPW resonator designs.

4.5 Fabrication results

This section is divided in two parts, the laser lithography results (before pattern transfer), and after pattern transfer plus photoresist removal. As previously discussed, outcomes are based on design in chapter 3. Corresponding to chips of Al (100 nm) + Si (500 μm). Images, or micro-graphs, are taken by the optical microscopy (OM) and the scanning electron microscopy (SEM).

4.5.1 Before pattern transfer

Some exposure conditions tests have been done to determine which exposure conditions allow optimized outcomes. In this subsection the fabrication results after light exposure, are shown. In figure 4.6 is presented the interdigitated finger 2+2 capacitor dimensions, changing modulation and writing velocity parameters. As observed, the best conditions are obtained when, 15 % modulation and 2 mm/s writing velocity, finger capacitors are used (also shown previously, in Table 4.1).

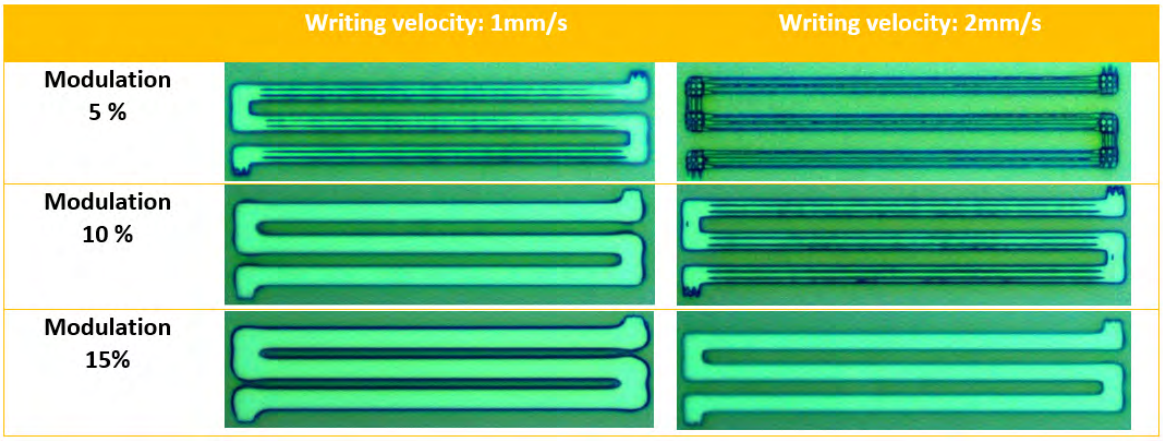

Figure 4.6: Different finger 2+2 capacitors, changing the modulation and writing velocity of the laser writer.

As mentioned, the dimensions of finger electrodes are very close to the nominal resolution of the 1 μm laser spot. Fine tuning required a study of the number and separation of trajectories. Figure 4.7 displays how affect laser trajectories for fixed exposure parameters. In this case, as previously mentioned in figure 4.4, the best situation is using three laser trajectories, with 1 μm separation between each one.

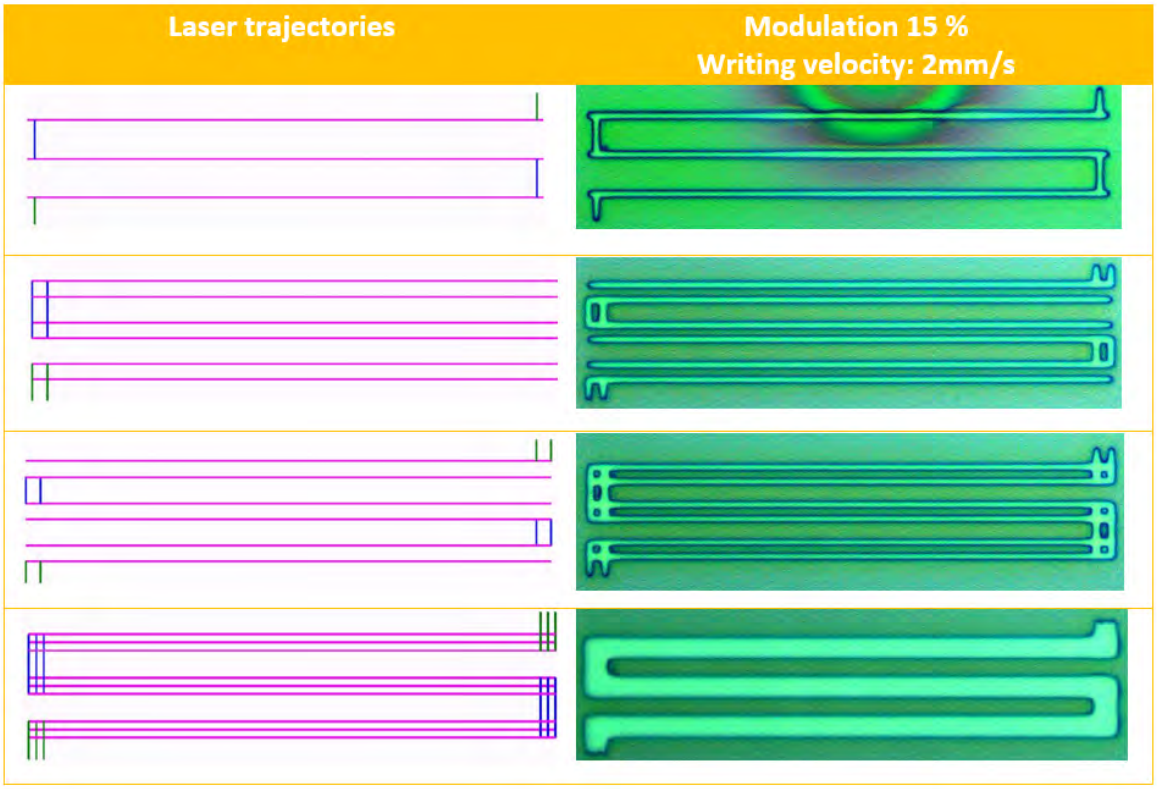

Figure 4.7: Different finger 2+2 capacitors changing the number of laser trajectories.

As for the whole structure, additional issues were found. We have determined that, after deposition, the exposure and next steps have to be implemented after waiting, at least, 12 hours. More details are given in Annex D.

Figures 4.8 and 4.9, shows the outcomes obtained in laser lithography, before the wet etching process and photoresist removal. In figure 4.8, the critical parts of the CPW resonator are presented by the use of OM (x50). And figure 4.9 displays a general view of the CPW resonator, also by the use of OM (x5). The pattern accuracy and resolution obtained are very close to the ones showed in chapter 3. Therefore, we decided to proceed with the pattern transfer.

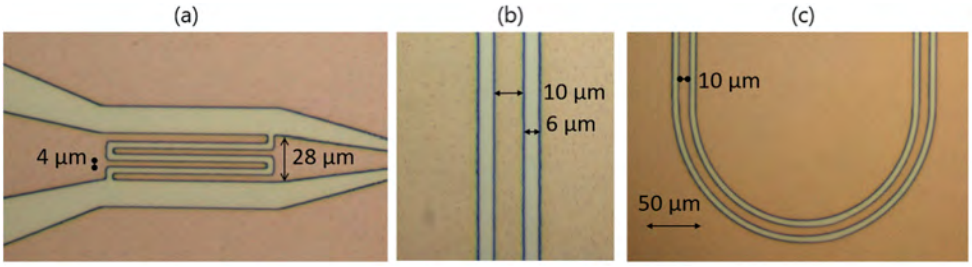

Figure 4.8: Images (before pattern transfer) made by OM (x50). (a) 2+2 finger capacitor (b) and (c) captures of the meanders.

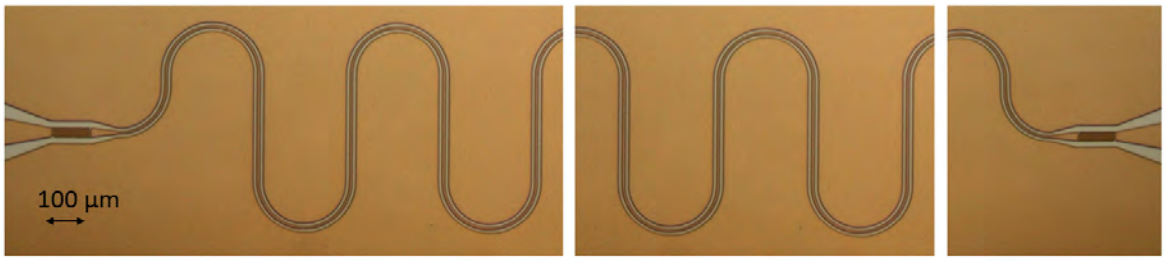

Figure 4.9: Image of the CPW resonator (before pattern transfer) made by OM (x5), in the cleanroom, at IMB-CNM.

4.5.2 After pattern transfer

In this section, the results, after wet etching process and photoresist removal, are shown. This two steps have been implemented by specialist engineers from IMB-CNM, due to safety and previous experience was required to do it. These are the two last steps of the whole process presented, previously, in Figure 4.1.

Figures 4.10 and 4.11 displays the critical parts of the CPW resonator. In figure 4.10, a image taken with SEM [1] is given for a finger capacitor composed by 100 nm thickness Al and 500 μm thickness Si (intrinsic).

[1] SEM images were taken by Gemma Rius.

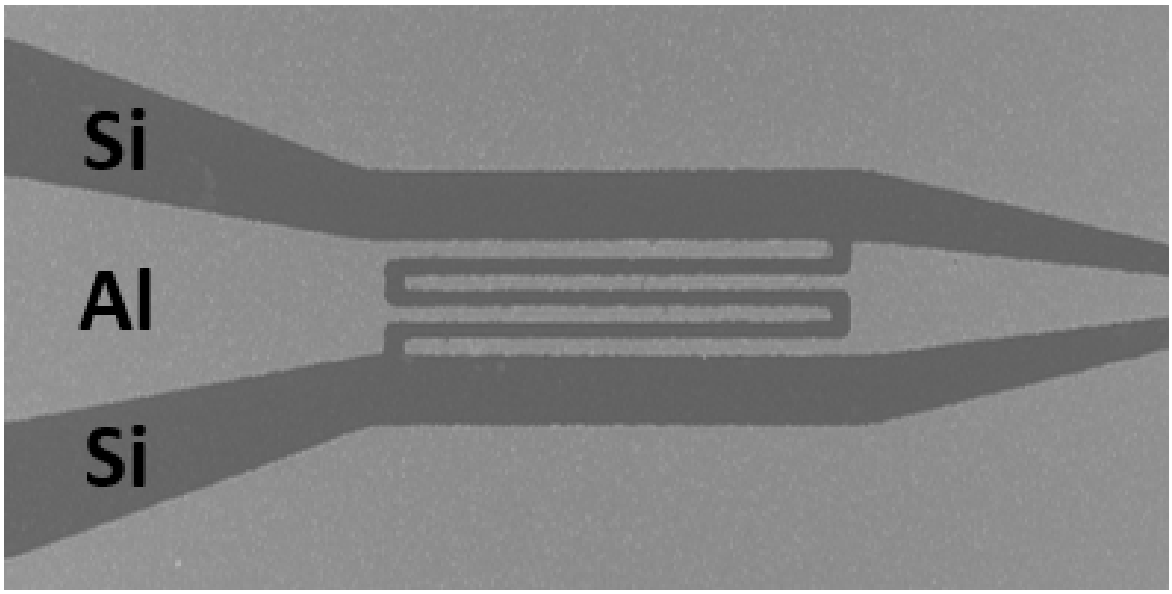

Figure 4.10: Image of 2+2 finger capacitor (after pattern transfer), taken with SEM.

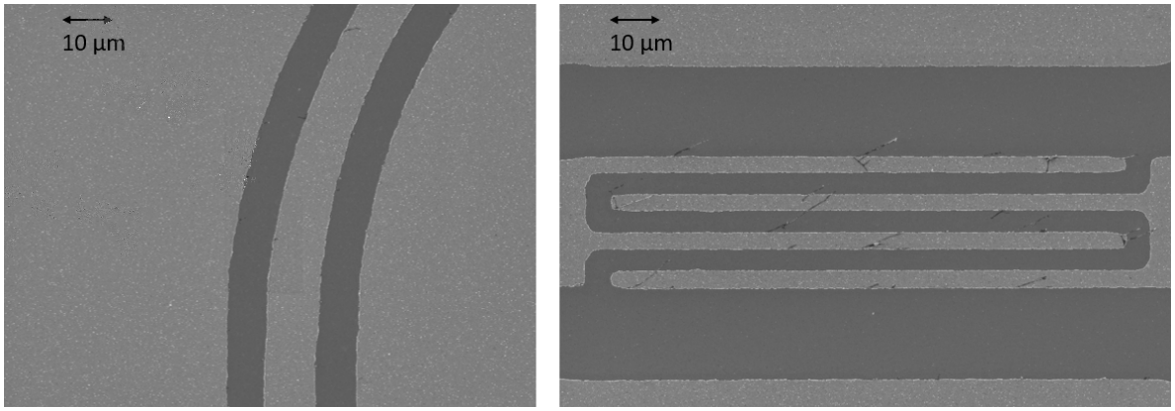

Figure 4.11: Images (after pattern transfer) taken with SEM. (left) part of a meander; (right) 2+2 finger capacitor .

In figure 4.11 has been corroborated that the dimensions of the smallest parts in the CPW resonator are preserved upon pattern transfer by wet etching. The dimensions are equivalent to the results obtained in the previous subsection 4.5.1, in figures 4.8 and 4.9, and consequently also with the design discussed in chapter 3.

A general overview of the full resonator composed by different images is presented in figure 4.11.

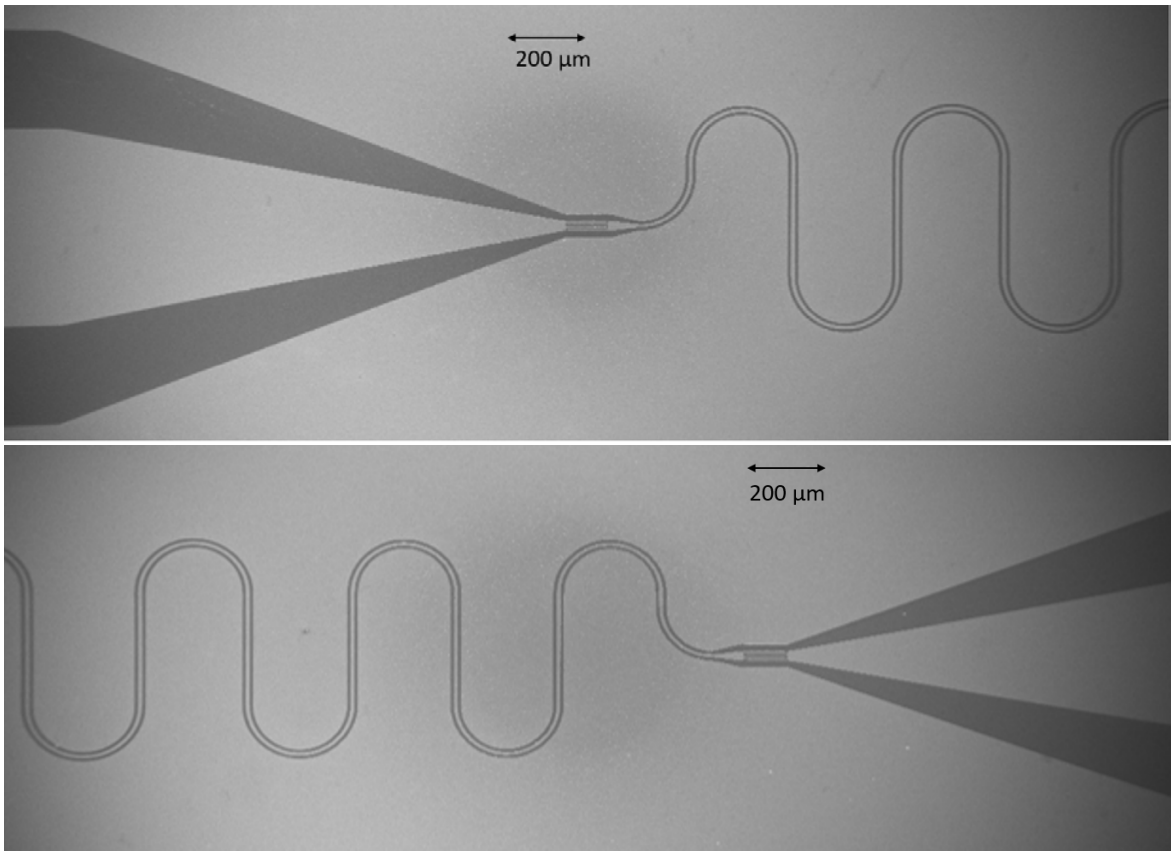

Figure 4.12: Overview images (after pattern transfer) taken with SEM, of the CPW resonator.

As a conclusion for this fabrication part, a processing sequence has been validated and processing conditions have been determined. First prototypes have been successfully generated and could be tested for its operations/functional purpose. Specifically, the fabrication results observed, have a quite precise resolution for the most critical parts, such as curved meanders, or single-digit micrometer dimensions of the finger capacitors. Definite validation of the resonator development would be the measurement in the cryogenic refrigerator to see how differ the theoretical results and dimensional structures with the measures.

Chapter 5

Conclusion

This Master Final Thesis has addressed the design, simulation and fabrication of superconductor coplanar waveguide resonators for their application in quantum computing.

An extensive study on the theory of superconducting resonators is presented, paying special attention to the design of transmission line resonators. The circuit is based on the materials (Si and Al) and geometry (coplanar waveguide - CPW), and we have explained how loss tangent of Si take over the loss of the circuit. Simulations were analyzed with Sonnet Software. Several resonators have been tuned to operate from 6.4 to 6.9 GHz, and obtaining quality factors from hundreds to thousands (10^5). Two designs were selected for further developments, as follows. A first simulation design was presented, showing the transmission results, which has been the basis for the implementation in the fabrication process. In the second design, an in-depth study on coupling capacitance, changing the type of capacitors (finger or gap) has been done. In particular, the dependence between the coupling capacitance and the quality factor was considered. Then, the transmission losses were analyzed by the coupling capacitance, introducing the terms of critical coupling, and how the resonator can be in an overcoupled or undercoupled regime, and which are the implications for each. Additionally, the dependence between the resonant frequency and the coupling capacitance has been analyzed and how elements, coupled to the transmission line resonator, can shift the resonant frequency. Finally, how the quality factor affects the harmonic modes, studying the effect of the reflection and transmission parameters, has been studied.

Experimentally, the results of the fabrication process based on the first simulation design are presented. Firstly, the processing sequence is defined and described. It is based on optical lithography and a wet etching process. This work introduced a new laser writer photoresist, i.e. preliminary tests to optimize particularly smallest elements were needed. Generation of CPW resonator layout and preparations for laser writer implementation required specific work. Specifically, GLADE software was used for generating the layout structures, and KLOE design software to manage the photolithographic process. The importance of converting the different layout elements into the laser trajectories has been highlighted, as well as how the exposure parameters, such as modulation or writing velocity, play an important role in achieving the accurate dimensions. Optimal exposure values have been determined, for each structure, as illustrated with the results images of the obtained patterns. Finally, the first superconducting CPW resonator fabrication has been completed.

As a concluding remark, at this point, the real devices could be tested to evaluate their performance and the agreement with the simulation results, which due to time and confinement issues has not been possible, unfortunately, during this thesis research period.

Appendix A

Extension of Transmission line theory

A.1 Lumped-element circuit model for a TL

Previously commented in chapter 2, a TL normally is approximated as a two-wire line. In terms of analyzing these circuits, can be approximated through what is called, the lumped-element circuit (see figure A.1), which considers that an infinitesimal length Δz, in that TL, is a set of series and parallel parameters[27]:

- **Resistance (R)**: series resistance per unit length, for both conductors, in Ω/m units. This parameter is limited by the finite conductivity in the conductors. (Note that in case of superconductivity $R = 0$)
- **Inductance (L)**: series inductance per unit length, for both conductors, in H/m units. This parameter comes from the total self-inductance of the conductors, also it is defined as the ratio between the magnetic flux and the electric intensity.
- **Conductance (G)**: shunt conductance per unit length, in S/m units. Due to dielectric loss in the materials.
- **Capacitance (C)**: shunt capacitance per unit length, in F/m units. This term is caused by the proximity of the conductors, in a TL, storing electric energy.

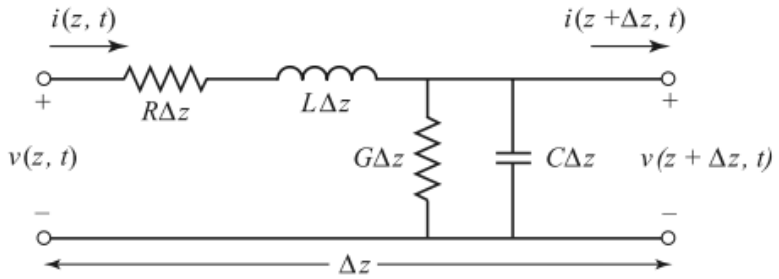

Figure A.1: Lumped-element model for a transmission line [27].

Applying Kirchhoff's rules in figure A.1 to voltages $V(z,t)$ and currents $I(z,t)$:

$$v(z,t) - R\Delta z \cdot i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(\Delta z + z, t) = 0, \tag{A.1}$$

$$i(z,t) - G\Delta z \cdot v(\Delta z + z, t) - C\Delta z \frac{\partial v(\Delta z + z, t)}{\partial t} - i(\Delta z + z, t) = 0. \tag{A.2}$$

Considering $\Delta z \to 0$, equations A.1 and A.2 can rewritten as:

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t}, \tag{A.3}$$

$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t}, \tag{A.4}$$

called the Telegrapher Equations.

Applying equations A.3 and A.4 for the sinusoidal steady-sate condition, with cosine-based phasors [27]:

$$\frac{\partial V(z,t)}{\partial z} = -(R + j\omega L)I(z), \tag{A.5}$$

$$\frac{\partial I(z,t)}{\partial z} = -(G + j\omega C)V(z). \tag{A.6}$$

A.2 Propagation on a Transmission Line

Equations A.7 and A.8 give traveling wave solutions to equations 2.1-2.2, presented in chapter 2.

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}, \tag{A.7}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}. \tag{A.8}$$

Where voltage and current can be seen as a two plane waves travelling in opposite directions. $e^{-\gamma z}$ displays a wave travelling through the +z direction and $e^{\gamma z}$ a wave travelling through the -z direction. Applying A.5-A.6 to A.7-A.8, the characteristic impedance Z_0:

$$Z_0 = \frac{R + j\omega L}{\gamma} = \frac{R + j\omega L}{G + j\omega C}. \tag{A.9}$$

And

$$\frac{V_0^+}{I_0^+} = Z_0 = \frac{-V_0^-}{I_0^-}. \tag{A.10}$$

Wavelength λ of the line:

$$\lambda = \frac{2\pi}{\beta}, \tag{A.11}$$

where β is the phase constant, previously shown in equation 2.3, in chapter 2.
And the phase velocity v_{ph}:

$$v_{ph} = \frac{\omega}{\beta} = \lambda f \tag{A.12}$$

A.3 Lossless transmission line

The lossless transmission line simplification is justified since we use lossless materials (superconductors) and high quality dielectrics with very low dielectric loss tangent. Considering a lossless TL, $R = 0$ and $G = 0$. The propagation constant (equation 2.3) can be rewritten as:

$$\gamma = \alpha + j\beta = j\omega\sqrt{LC}, \tag{A.13}$$

with

$$\beta = j\omega\sqrt{LC}, \tag{A.14}$$

$$\alpha = 0. \tag{A.15}$$

Thus, the characteristic impedance:

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{A.16}$$

The voltages and currents on lossless TL:

$$V(z) = V_0^+ e^{-j\beta z} + V_0^- e^{j\beta z}, \tag{A.17}$$

$$I(z) = \frac{V_0^+}{Z_0} e^{-j\beta z} - \frac{V_0^-}{Z_0} e^{j\beta z}. \tag{A.18}$$

The phase velocity is given by:

$$v_{ph} = \frac{1}{\sqrt{LC}} \tag{A.19}$$

A.4 The terminated transmission line

A fundamental property of distributed elements happens when the device is connected to a power source. To do that we need to ensure that all power delivered is not reflected for your circuit inducing undesired effects. These effects can be avoided by putting a load impedance Z_L at the end of your TL (fulfilling $Z_L = Z_0$). Otherwise, Z_L becomes the ratio voltage-current at the load [27]. Figure A.2 shows the lossless TL model of an arbitrary Z_L.

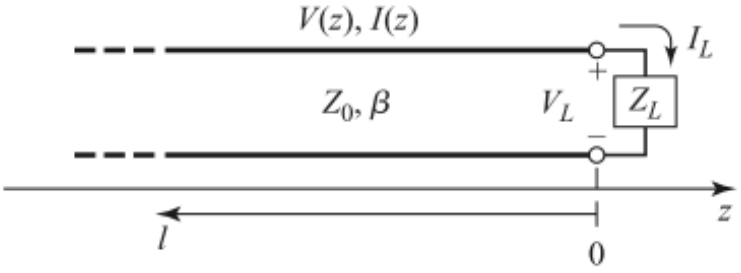

Figure A.2: A transmission line terminated in a load impedance Z_L [27].

Applying expressions A.17-A.18 to an arbitrary load impedance Z_L at $z = 0$:

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_0^+ + V_0^-}{V_0^+ - V_0^-} Z_0. \tag{A.20}$$

Solving A.20, the reflection coefficient can be expressed as:

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{A.21}$$

Equation A.21 shows that no reflected parameters $\Gamma = 0$ when $Z_L = Z_0$. Also, equations A.17-A.18 can be rewritten as equations 2.4-2.5, in chapter 2.

Thus, the reflection coefficient affects to the average power flow P_{av} along the line:

$$P_{av} = \frac{1}{2}[V(z)I(z)^*] = \frac{1}{2}\frac{|V_0^+|^2}{Z_0}(1 - |\Gamma|^2). \tag{A.22}$$

P_{av} is constant at any point on the line, and is maximum when $\Gamma = 0$.

Equation A.21 shows how the reflection coefficient look like at $z = 0$. Nevertheless, a generalized equation for Γ can be rewritten to any point l, with $z = -l$

$$\Gamma(l) = \frac{V_0^- e^{-j\beta l}}{V_0^+ e^{j\beta l}} = \Gamma(0) e^{-2j\beta l}. \tag{A.23}$$

Also, the input impedance Z_{in} can be define at a distance $l = -z$ from the load:

$$Z_{in} = \frac{V(-l)}{I(-l)} = Z_0 \frac{V_0^+(e^{j\beta l} + \Gamma e^{-j\beta l})}{V_0^+(e^{j\beta l} + \Gamma e^{-j\beta l})} = Z_0 \frac{1 + \Gamma e^{-2j\beta l}}{1 - \Gamma e^{-2j\beta l}} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)}. \tag{A.24}$$

The last expression corresponds to the one in equation 2.8, discussed in chapter 2.

A.5 Microwave network analysis: Scattering matrix

Sonnet software [26] simulations are described by the Scattering parameters [27][1]. Direct measuring involve the magnitude and phase of the wave traveling in a given direction when measuring voltages and currents at MW frequencies. A way of dealing with direct measurements is the Scattering matrix [27]. A general expression of scattering matrix:

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \dots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & S_{22} & \dots & S_{2N} \\ \dots & \dots & \dots & \dots \\ S_{N1} & \dots & \dots & S_{NN} \end{bmatrix} \cdot \begin{bmatrix} V_1^+ \\ V_2^+ \\ \dots \\ V_N^+ \end{bmatrix} \tag{A.25}$$

A.25 represents Scattering matrix of a N-port network. Where V_n^- is the voltage wave amplitude reflected from port n and V_n^+ the wave amplitude incident. The Scattering matrix is defined as a relation to these reflected and incident parameters [27]. Additionally, the elements S can be determined as[2]:

$$S_{ij} = \frac{V_i^-}{V_j^+}\Big|_{V_m^+ = 0; k \neq j} \tag{A.26}$$

These elements S_{ij} are found by driving port j with an incident wave of voltage V_j^+ and measuring the reflected wave amplitude V_i^- coming out of port i; all other ports are terminated in matched loads to avoid reflections.

In particular, the case presented for a CPW resonator, in this project, correspond with a 2-port network. So expression A.25 can be rewritten as A.27.

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{A.27}$$

Figure A.3 displays the model of a 2-port network. Note that the network must be connected to load impedances Z_L.

[1] Experimentally, vector network analyzer (VNA) is used to analyze scattering parameters

[2] i,j $\in \{1, 2, 3, \dots\}$

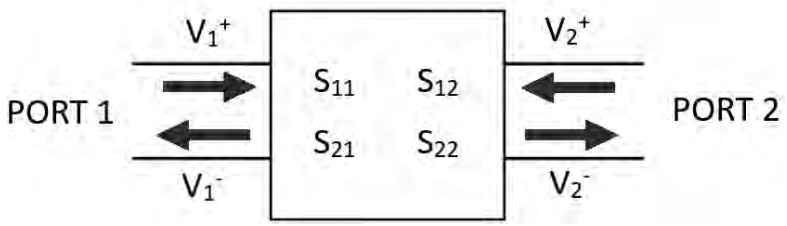

Figure A.3: 2-port network to represent the scattering parameters for the CPW resonator.

In the case presented in this project, since the CPW resonator is symmetrical: $S_{11} = S_{22}$, and $S_{12} = S_{21}$. Simulations results presented in chapter 3, shows the outcomes achieved in dB units. So the correct expression is given by:

$$S_{ij}(dB) = -20\log(S_{ij}). \tag{A.28}$$

Appendix B

Tests simulations

This appendix is divided into two sections: an extension of the resonator and the capacitor simulations.

B.1 Extension of the resonator simulations

This section presents additional tests of the optimized resonator design. The differences between the first and the optimized design are not many in terms of transmission or quality factor parameters. The improvements achieved are the size of the chip and consequently the time of simulation in Sonnet Software (from 30h to less than 1h 30 min).

Sonnet gives the possibility to simulate currents depending on the frequency. The following figure B.1 shows an example of how the first two harmonic modes behave in terms of current density. If figure B.1 is compared with figure 2.3 (chapter 2), a theoretical validation of current density simulations is done by the distributions between maximums and minimums.

During the project some designs were proven testing different properties of the geometry. Concerning the transmission line, preliminary tests with the rectilinear TL were analyzed, however once suitable outcomes were obtained, meanders were tested. During the simulations, multiple problems have appeared as the circuit was optimized. From the beginning, attempts have been made to design the chip as small as possible while preserving the conditions that should be obtained by comparing them with various bibliographic sources [15, 16, 18, 28].

1. **Dielectric properties**: fundamental since dielectric losses limit the resonator's internal quality factor.

2. **Width of GND planes**: The width of the GND planes is fundamental to isolate the circuit from other unwanted energy sources. They must be at the same voltage to achieve the expected results, considering the width of GND planes greater than $\lambda/10$ [32].

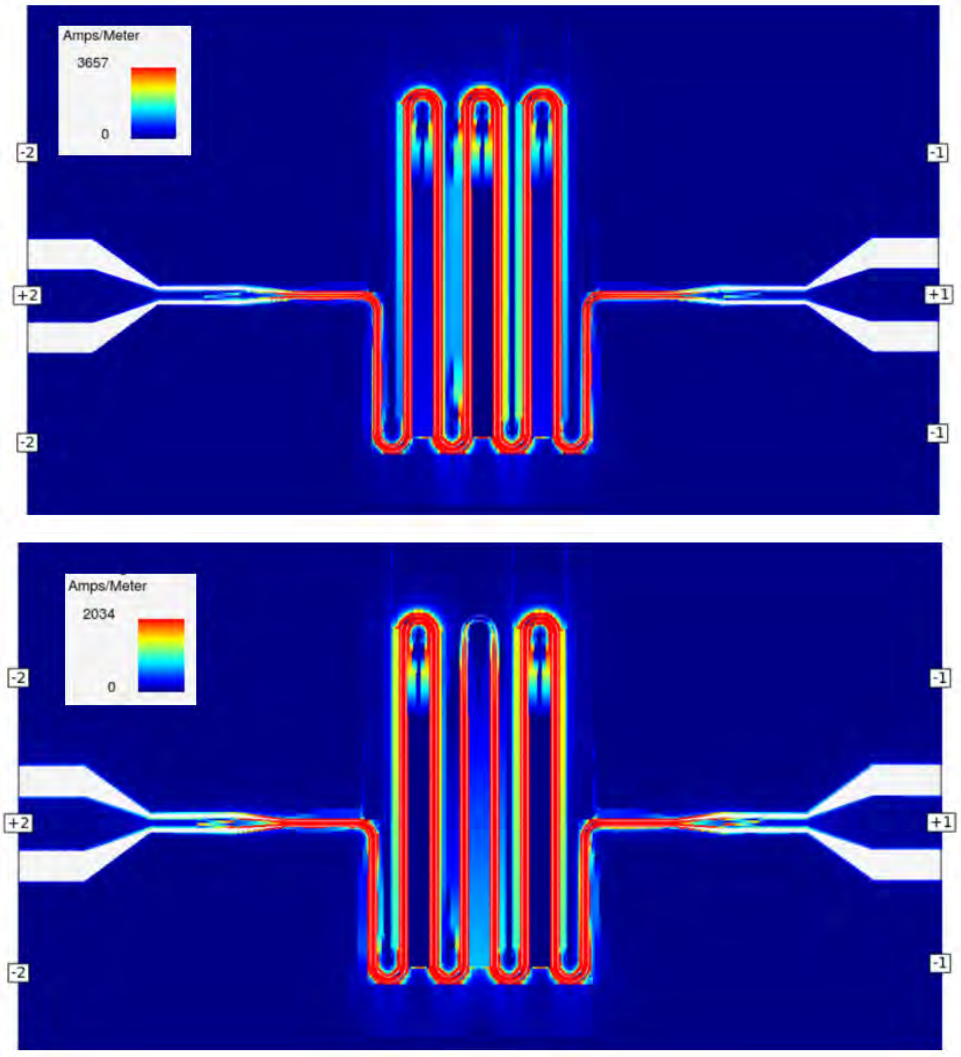

Figure B.1: Current distribution of first two harmonic modes in the CPW resonator (optimized design) with two symmetrical 2+2 finger capacitors. Capture taken from Sonnet software.

3. **Coupling connectors and capacitors**: The coupling of the different structures is essential when preserving the properties of the system. To do this, it is necessary to increase the W/S ratio while maintaining $Z_0 = 50$ ohms.

4. **Meshing and simulation time**: Sonnet uses cell sizes to simulate the different structures of the circuit, therefore it is essential to optimize the minimum cell size as much as possible along with the number of cells. Meshing, consequently, in Sonnet, depends on the simulation time. The smaller the cell size, more accurate results but also longer simulation time. So a proper meshing must be done in order to have consistent outcomes. In this project, 2x2 μm cell sizes were used.

5. **Six-sided metal box**: Further tests were made, at the end of the project, in order to see how the circuit behaves in a six-size metal box. Note that, as presented in chapter 3, the circuit had free-space covers to avoid box resonances. Figure B.2 (above) shows how considering metal (lossless) covers, the circuit creates unwanted transmission resonances; and secondly (below) the possibility to eliminate them, by creating vias to a ground plane under the silicon layer, which

avoids possible changes in the ground potential, as geometry in figure B.3 displays.

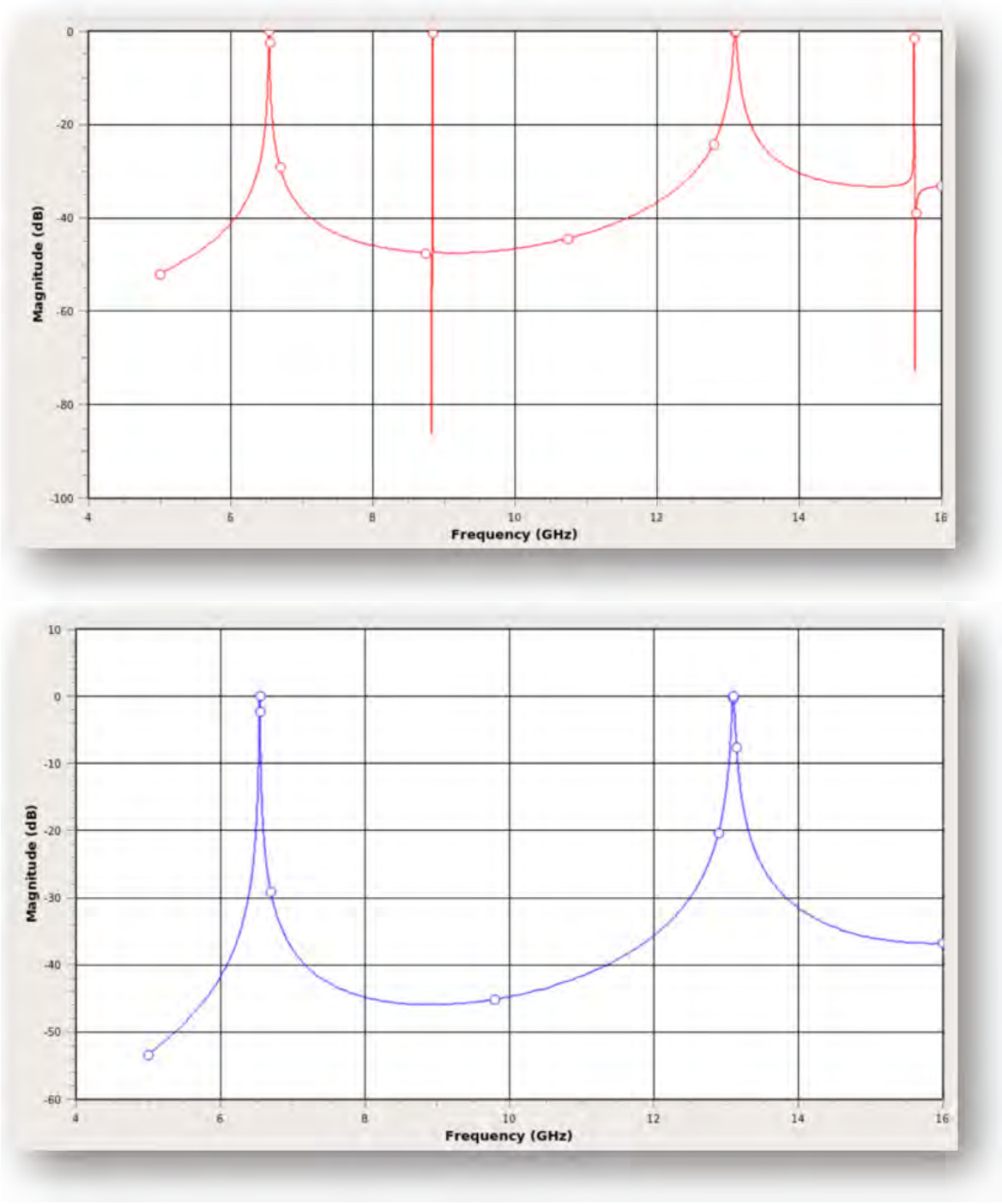

Figure B.2: S_{21} distribution of first two resonant frequencies, for a six-sided metal box (optimized design) with two symmetrical 2+2 finger capacitors. At the top, red line for the CPW resonator . At the bottom, blue line for the CPWG resonator (figure B.3). Capture made in Sonnet software.

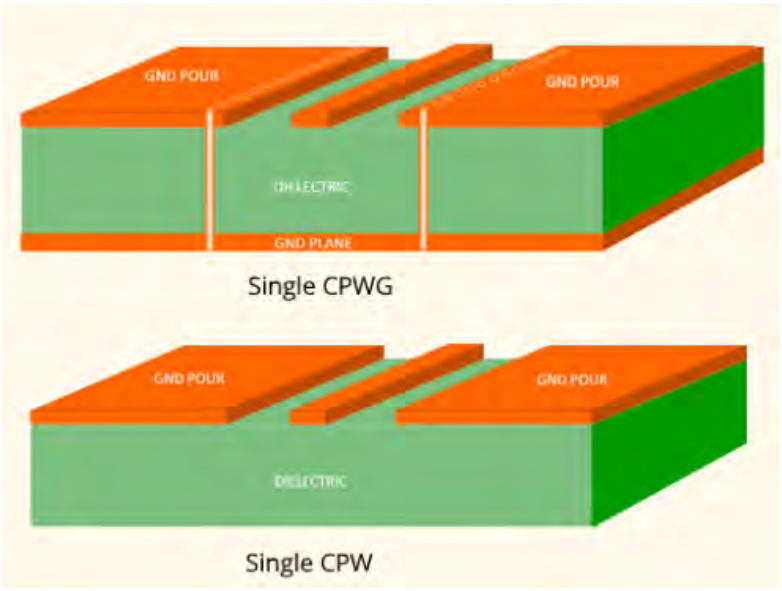

Figure B.3: Coplanar waveguide geometry. Above CPWG, below CPW.

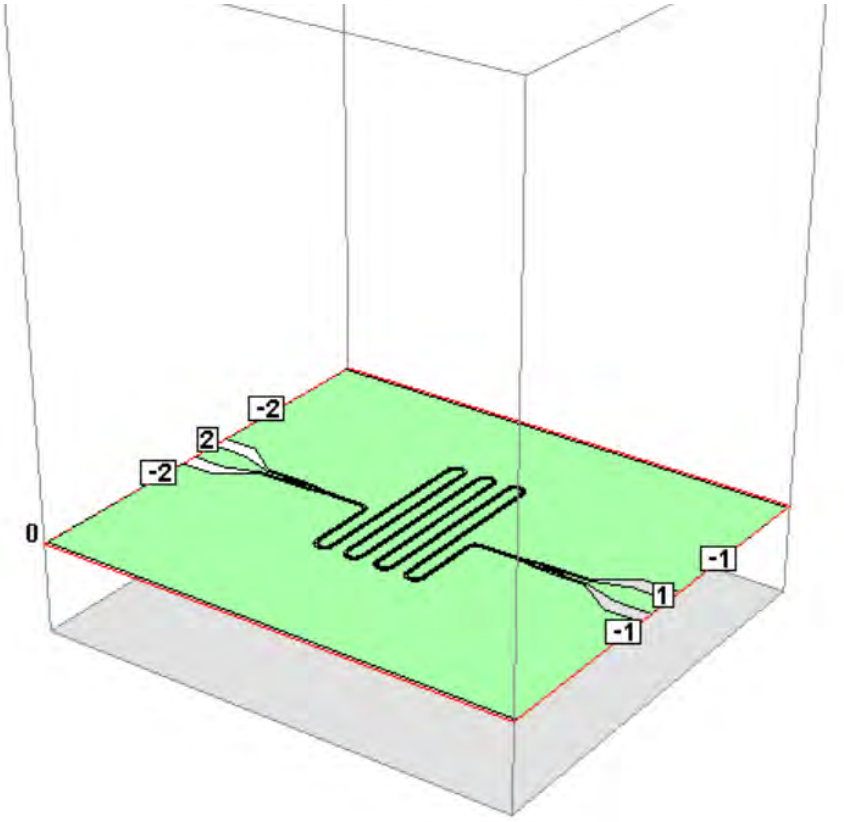

Figure B.4: 3D top representation of a six-sided metal box for simulating the superconducting CPW resonator (optimized design).

B.2 Capacitor simulations

Applying a PI-model in Sonnet [26] (figure B.5), the value of the coupling capacitances are obtained, for the symmetrical CPW resonators, presented in chapter 3.

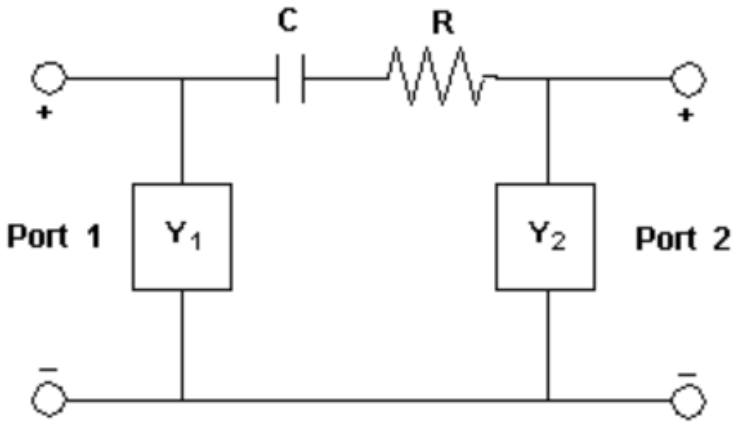

Figure B.5: PI-model used to measure the capacitance between two ports in sonnet software.

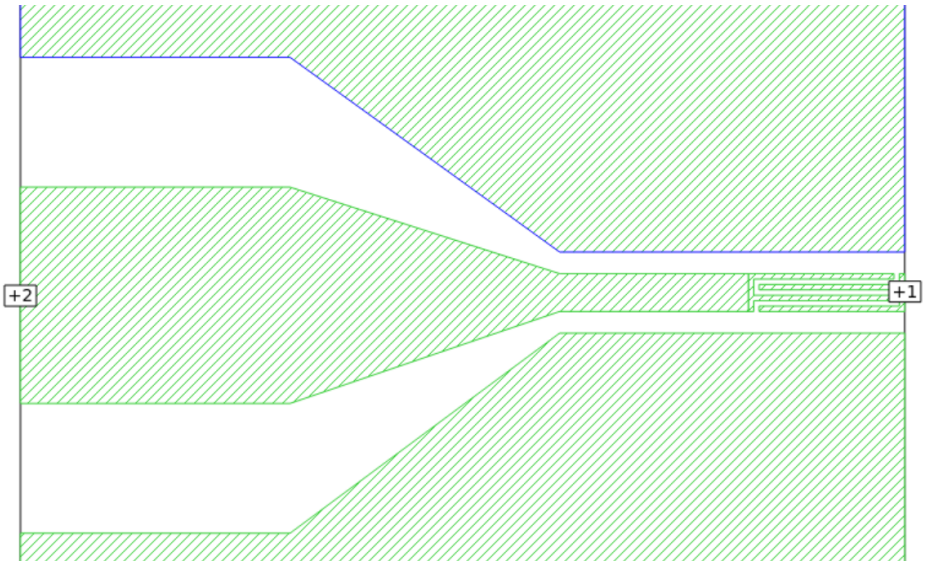

Figure B.6: Geometry used for capacitance measurements (PI-model) in the interdigitated 2+2 finger capacitor. Capture taken from Sonnet software.

The different results, for the different capacitors (see Table 3.5 in chapter 3) are in agreement with expected theoretically, with a maximum standard deviation $\sigma(C_k) = 1.35 fF$ for a finger 3+3 capacitor.

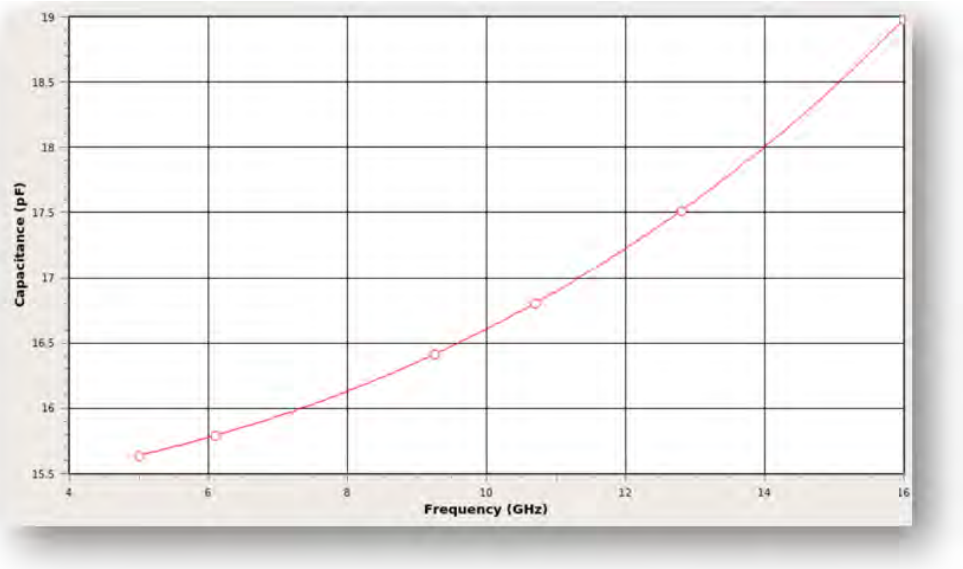

Figure B.7: Representation of capacitance using a PI-model, measurement for a interdigitated 2+2 finger capacitor. Capture taken from Sonnet software.

Appendix C

Photolithography process

Photolithography is the process of transferring a design pattern to the surface of a wafer. This process is an essential and often most critical process in the semiconductor industry. Precisely, ultraclean conditions during wafer manipulation and processing, for the prevention of particle contamination and light filtration, are requisite. In that sense, IMB-CNM Clean Room, where has been made this process, has a Class 100 in the rating by Class Effectiveness of Filtration. Class 100 ensures a maximum number of $0.5\mu m$ and $5\mu m$ particles size per m^3 to be below 3500 and 230. Figure C.1 shows the several steps in a typical photolithography sequence.

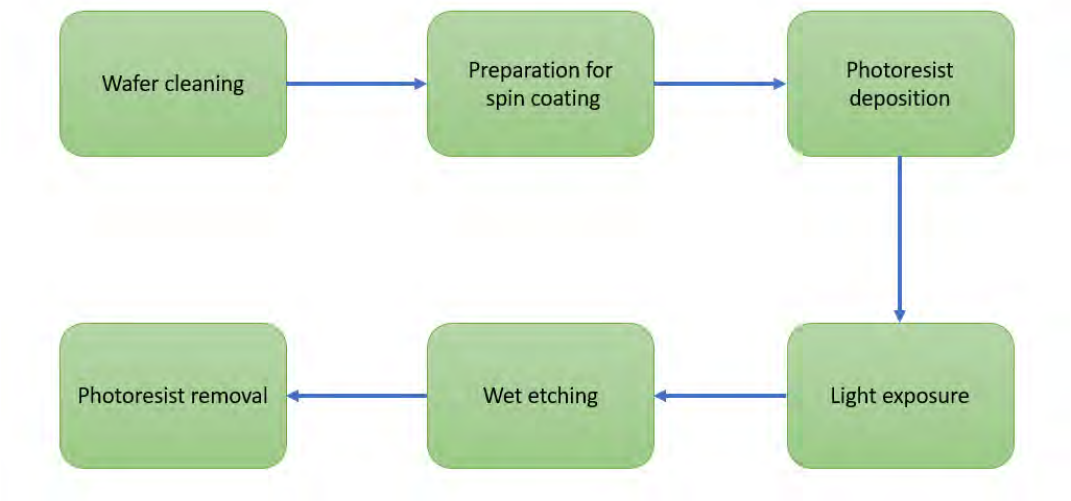

Figure C.1: Steps of a photolithography process.

In addition to the light exposure, photolithography process typically consists in: wafer cleaning, adhesion promoter step, photoresist deposition by spin coating, soft bake, light exposure, development and photoresist removal. In some cases, after exposure and depending on photoresist type, it might be necessary a post-baking, or also called hard bake, however, it was not needed in our case (S1805 positive photoresist). More details for each step are given below.

C.1 Wafer preparation and dehydrating

The chips used are $1.2x1.2cm^2$ approximately. In this project, the standard cleaning process [23] was applied. It consists in:

- Wafer immersion in electronic grade acetone for 5min to clean the surface from organic contaminants. Usually ultrasonication is added to the treatment for better cleaning.
- Immersion in electronic grade isopropanol for 5min to remove the remaining acetone rests.
- Rinsing in deionized water for 1min.
- Drying with N_2 gun.

C.2 Primer treatment

To remove any water or solvent molecules absorbed in the surface two steps are often used:

- Bake: 10 min in hot plates at 120 ºC.
- HMDS deposition: particularly, the program 2 defined by IMB-CNM Clean Room engineers.

C.3 Photoresist deposition

A resist thin film is used for photolithography, which thickness can be precisely determined by using the spin coating technique. The positive photoresist used is called S1805. The deposition of a photoresist onto the wafer is done in a liquid form, where the use of pipettes is recommendable. This resist is UV light-sensitive so is essential to work in an environment with UV filters to avoid undesired resist exposition.

The wafer/chip is placed in the spinner Delta 20 FLI8, fixed on vacuum chuck. And after verifying proper vacuum, the chip is ready to be spinned at high speeds. In particular, it is used the program 7, which is based on 5 steps with different spin velocities in the range of 1000-5000 rpm during around 1 min and a half, and resulting in a photoresist thickness of 400 nm [1].

[1] The actual thickness of the resist depends on its viscosity and is inversely proportional to the square root of the spinning speed.

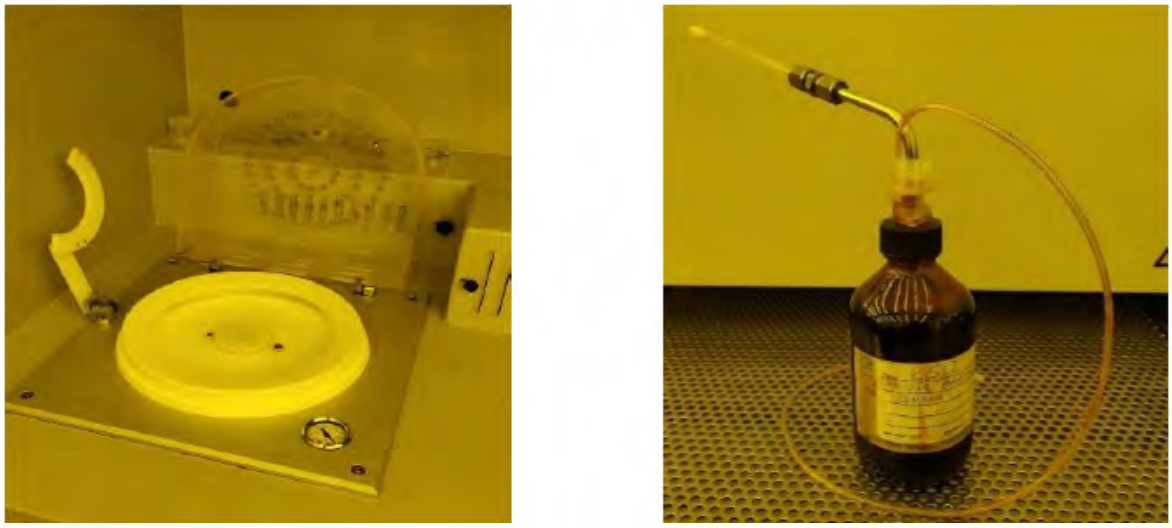

Figure C.2: On the left Delta 20 FLI8 spinner, and on the right Hybrid S1805 photoresist.

C.4 Soft bake

A thermal heating procedure, as previously used in the substrate step, needs to be done to improve photoresist adhesion on the wafer and remove excess of solvent. For the S1805 photoresist the wafer must be baked onto the hot plate (see figure C.3) at 115 ^{o}C for 1 min. At this point, the wafer is ready to be exposed.

Figure C.3: Hot plates in the Clean Room.

C.5 Light exposure

As previously discussed, the photoresist is UV light-sensitive so depending on the type (positive or negative tone) the areas exposed to the laser beam will behave differently upon development (see figure C.4). In the case of negative tone resist, design exposed

areas remain, reversely, in case of positive resists, exposed areas are removed upon development.

In our case, we used a **positive** resist S1805, which is an organic polymer which changes its chemical structure when it is exposed at wavelengths in the ultraviolet (UV) spectrum, from 10 to 400nm (we used 375 nm). Note that light absorption usually increases with shorter wavelength. Therefore, exposure needs to be selective to create the desired resolution wanted in each structure. In our case, the feature dimensions are in the order of 500 μm to 4 μm, so accurate designs of laser trajectories and calibration exposure conditions are crucial for the smallest elements (see chapter 4).

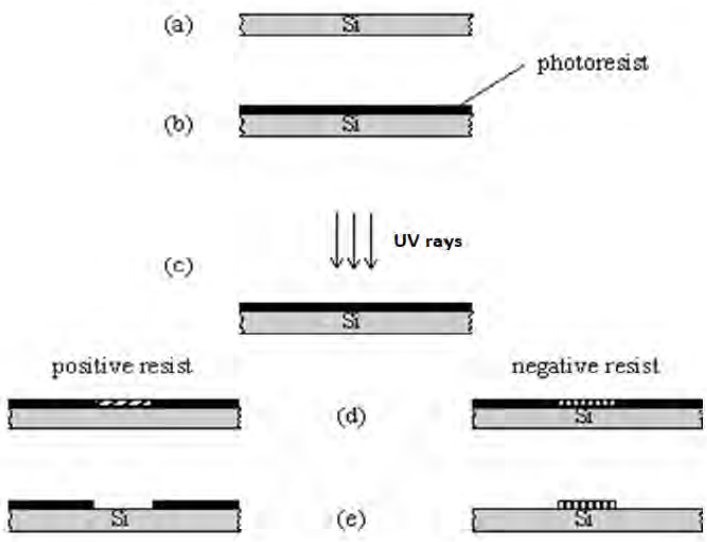

Figure C.4: Difference between positive and negative photoresist steps, in the photolithographic procedure [23].

C.6 Resist development

The patterns are revealed upon the so-called development step. The developer used is S1805 which causes the resist to swell and lose adhesion to the substrate. For safety issues gloves and special glasses are necessary to avoid skin contact with the compound, and also, laminar ventilation to breathe as little as possible the volatile molecules. The protocol used is:

- Immersion in S1805 developer for 10s to dissolve the exposed photoresist.
- Immersion in cascade for 15s to rinse, and stop the developer reaction.
- Immersion in distilled water for 15s to remove the remaining developer.
- Drying with N_2 gun.

Inspection of the patterned structures has been done on an optic microscope (OM).

Appendix D

Laser writing. Equipment and technology challenges

D.1 Equipment description

The Dilase 650 [40] is the model for the laser lithography system installed in the Clean Room at IMB-CNM. This system is a high-resolution direct laser system ($\approx 1\mu m$), able to operate at high scan speeds (up to 500mm/s) for generating flexible design of lithographic patterns even in thick layers (250µm to 10mm). The provided laser source is 375 nm wavelength (UV range). Moreover, the systems optic filters, homogenizes, and shapes the beam to reach and guarantee high resolution patterns. Specifically, the spot size, can be chosen as either $1\mu m$ or $10\mu m$ in diameter, while two objectives are available x10 and x40. In terms of the optics, the maximum resolution we can achieve after configured all parameters is $1\mu m$.

The laser scan to reproduce the patterns shapes. It is implemented by moving the sample stage, not the beam. The sample stage is the flat chuch that holds the sample with vacuum. The chip is moved in the X and Y axis (because the focal position is fixed[1]). Stage movement can reach up to 150mm x150mm. Placement of the patterns on the sample uses sample reference points, determined before laser exposure, by the user. A visualization camera is used to position it, with the aid of an white light, always taking care of not insolating the sample, with the white light in areas which are to be patterned. Table D.1 summarizes the maker specifications of the Dilase 650 equipment and figure D.1 a general overview of the actual equipment installed in the Clean Room.

Dilase 650 Laser writer	
Diode laser wavelength	375 nm
Optical line 1: laser spot size	$1\mu m$ (±250 nm)
Optical line 2: laser spot size	$10\mu m$ (±250 nm)
Lens enlargement	x10 or x40
Numerical aperture (N.A.	0.13 to 0.95

Table D.1: Specifications of Laser writer (650 Dilase) implemented in the cleanroom at IMB-CNM [40, 23].

[1]Movement in Z-axis, also known as focalization, is done and fixed always before launching the lithography process

Figure D.1: Overview of the Dilase 650 equipment implemented in the cleanroom at IMB-CNM

D.2 Operation sequence of laser writer

As previously discussed in chapter 4, there are some steps in order to use the laser writer. Firstly, the structure layout can be done, for example, with the software called GLADE (open-software). Once the file is exported as a ".gds" format to make it compatible with KLOE design software. Secondly, KLOE-design, requires conversion to laser trajectories of the polygons created in GLADE. And thirdly, Soft-Dilase 650, relies on specific beam steering. The full preparation of each software is detailed below.

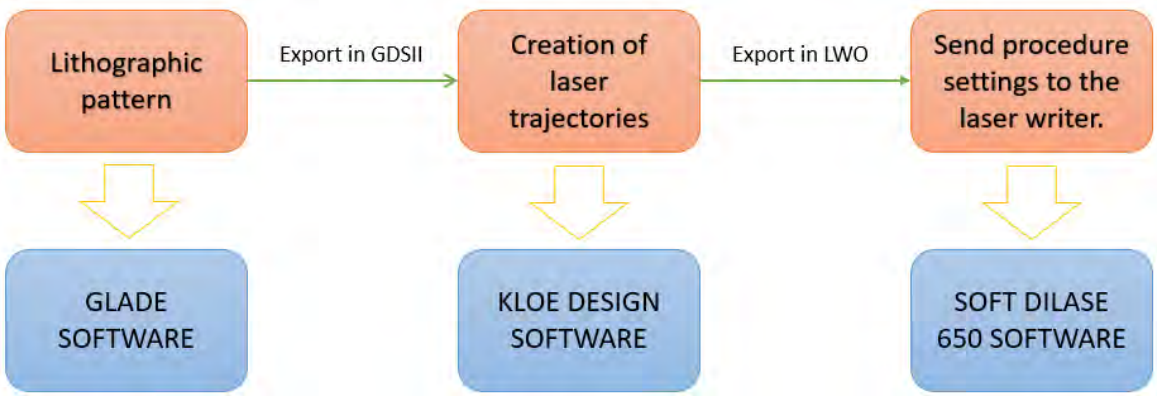

Figure D.2: Design implementation sequence.

List of actions and key aspects of **design** layer:

- Start importing the GDSII file from GLADE.
- Generate proper trajectories for the filling of each layout element/structure. In the case of connectors, horizontal filling was used, while for meanders vertical was used.

- The trajectories of finger capacitors have been generated manually as precisely-placed and accurate dimensionally-determined grids.
- Once created all trajectories, they are exported them in two separated ".lwo" files, one related to the large structures (meanders + connectors) and the second one related to high resolution capacitors.

Procedure and key issues of **Soft-Dilase 650 software**:

- Start the equipment by turning ON the main key switch and waiting until the start of the computer station is completed, and then running DilaseSoft.
- Open the front lid and place the resist-coated chip on the sample holder (chuck). Hold the chip by clicking vacuum button via the software (Point 5 in figure D.3). Sample stage needs to be initialized at this stage (Point 1 in figure D.3).
- Choose the spot size, 1 μm in our case (Point 2 in figure D.3).
- Set a reference point (origin) for the machine and proceed to define reference axes. Patterning alignment uses sample local coordinates. It is divided into two steps. The first one is choosing the focal length Z (distance between the sample and the objective or laser head.). This is a crucial step to get an optimum resolution, this length depends on the photoresist used (its thickness). The second one is choosing the reference point XY, which will be the point where the machine starts fabricating (Point 3 and 4 in figure D.3). By convention we use the left bottom corner of the wafer as our reference point.
- Now the two files ".lwo" can be imported into Dilase 650, and writing the exposure conditions such as modulation, velocity, position respect to the reference point and focal length. Note that is required to specify the laser spot size with the right-click mouse button in each ".lwo" file.
- Once these steps and exposure conditions are set, the process is ready to be implemented.

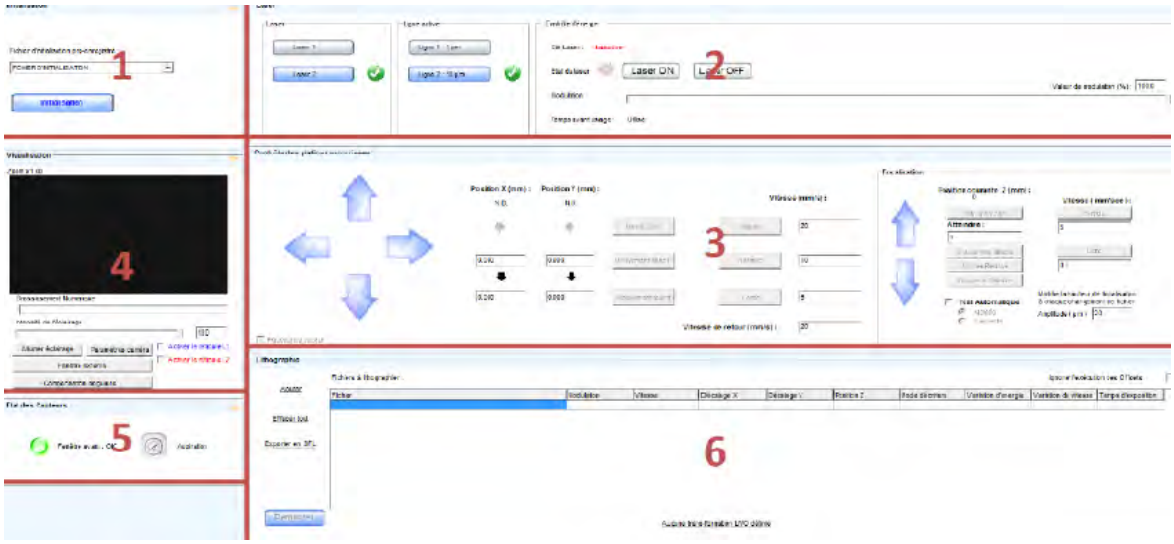

Figure D.3: Graphic interface of Soft Dilase 650 software for the exposure control panel.

D.3 Challenges and results of laser writing process

This work used, for the first time at the IMB-CNM, a resist for optimal laser writer application. A few issues have been encountered and overcome, as follows:

1. **Focalization (Z-axis)**: Determining the focal length between the laser writer and the sample is fundamental. This parameter is related to the thickness of both the photoresist and chip. The value is considered negative, in KLOE, due to the reference you are taking. Normally, in our samples the focalization is -0.068 mm, but it depends on the sample. And Z position is the sum between focalization plus a value -2.089 but would depend on the thickness of the photoresist. Not taking into account these parameters can lead in blurred (out of focus or poor resolution), such as shown in figure D.4.

2. **Cleaning process**: Remove any undesired particle on the chip surface is essential. Otherwise, the obtained pattern can be distorted or useless, as shown in figure D.5.

3. **Drying time**: We have determined that, after deposition, the exposure and following steps have to be implemented after waiting, at least, 12 hours. Otherwise, the results can lead to the ones presented in figure D.6 which are attributed to thermal or polymerization effects..

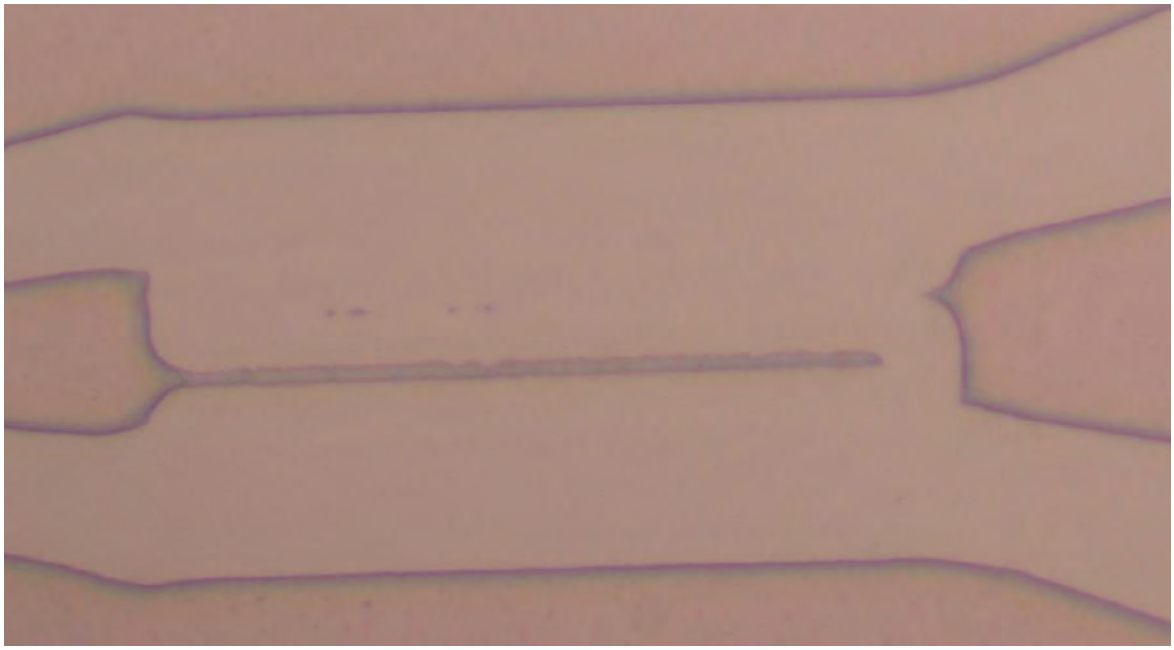

Figure D.4: Focus issue in the capacitor element. Captures taken by the optical microscope. It corresponds to finger 2+2 capacitor (x50).

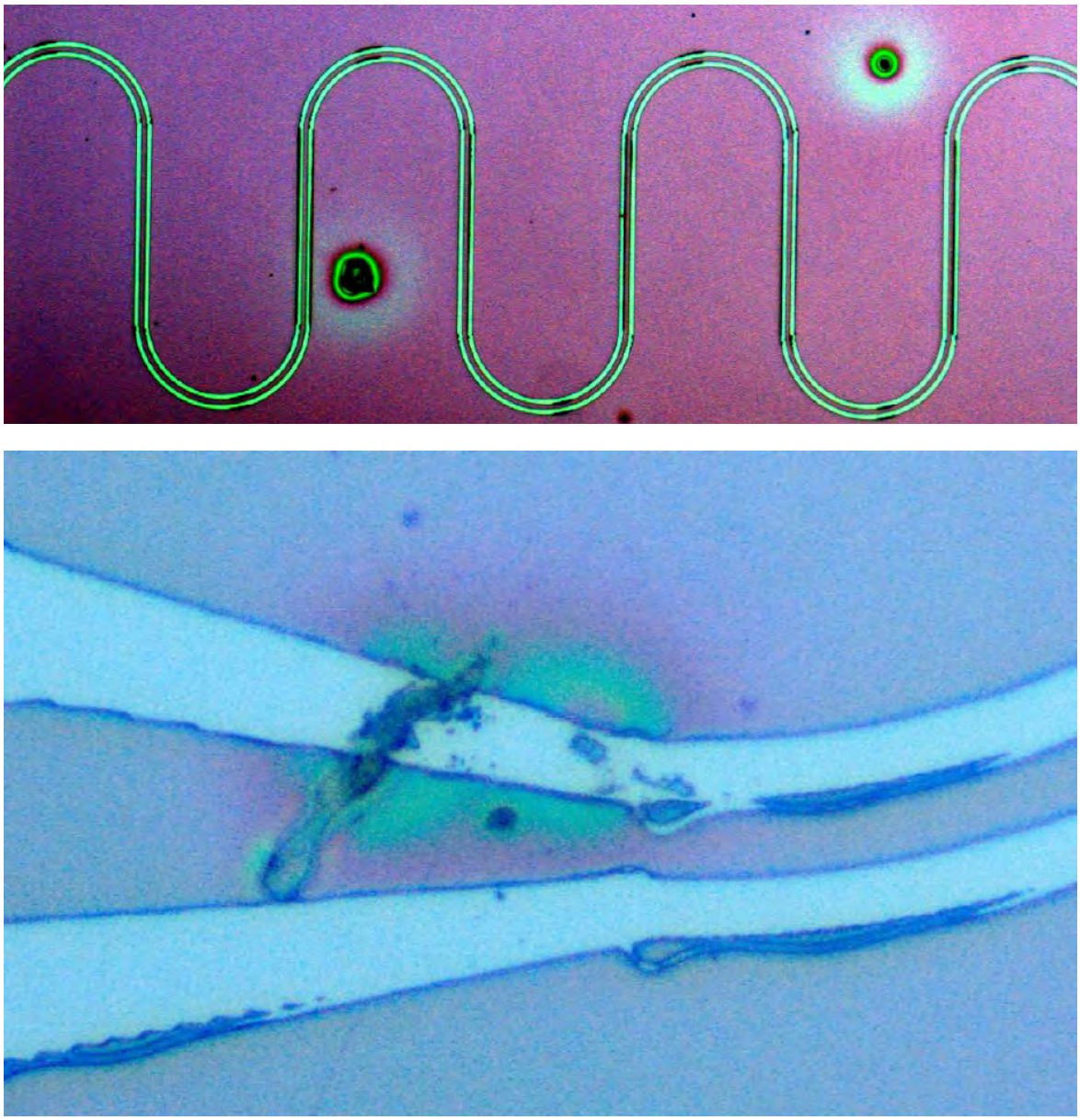

Figure D.5: Cleaning process issue in the CPW resonator. Captures taken by the optical microscope. Above, meander (x10); below junction between meander and finger capacitor (x50).

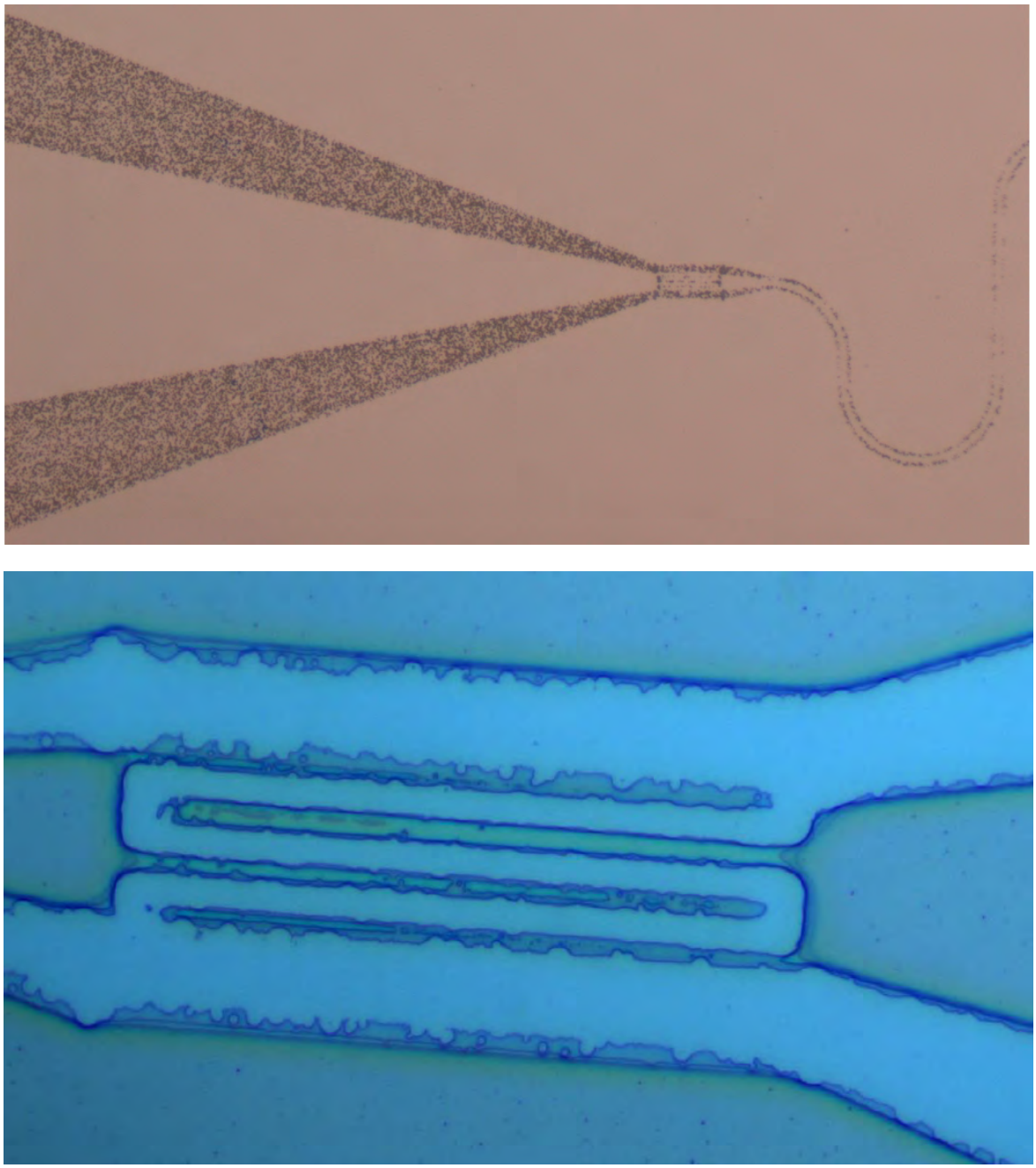

Figure D.6: Pots exposure writing time issue in the CPW resonator exposure. Captures taken by the optical microscope. Response of 1 hour of drying time. Above, connector and finger capacitor (x5); below finger capacitor (x50)

Appendix E

Context and state of the art

E.1 Presentation of topic

In the last 10 years, a lot of important advances have been made in the development of what is now known as the quantum computer prototype. Many research groups in quantum computers are popping up to lead the next great technological revolution of the next few years. But there are still several questions to be solved. Nowadays, the vision we have is that this technology will be complementary but not a substitute for a classic computer. Being possible, thanks to the quantum technology, to solve questions such as if these computers will be able to create completely secure communications, solve "unresolvable" algorithms or if they will be able to simulate behaviors of the matter, developing the new medicines of the future.

These questions, of course, will not be answered in this project, but it is expected that they can be answered in the coming years. This project focuses on creating superconducting circuits for coherent qubit-photon operations that will give us information about the interactions and their behavior, for in the future to become capable of designing a quantum processor.

E.2 Classical Computers

The beginning of this chapter can only begin by talking about the creation of the first replicas of classic computers designed by Alan Turing. This phenomenon, without a doubt, was a turning point in the way of thinking of a society that until that date saw impossible anything other than processing data through the nervous system of any living organism. This person, thanks to his invention in the middle of the second world war (1939-1945) helped to minimize the war (according to approximations) between 2 to 4 years, avoiding thousands of more deaths, solving the problem of the decision, helping to solve algorithms, deciphering crowd of cryptographic problems and above all helping to reflect on what we can do by forgetting conventionalisms and thinking differently.

From the invention of Turing, began to lay the foundations of what we know today as classic computers, that anyone today has in his pocket, at home, and work. These devices are called classics because they use processes by which humans can use logic, from simple mechanisms, to create algorithms or processes and decipher different types of mathematical, physical, or chemical problems among others, but of course

up to a certain limit. These are based on what is commonly known as a logical state or information bit, that is, on or off, alive or dead, 0 or 1. This being the starting point or starting point to create large and complex computational processes.

To manipulate these classic bits, it was necessary to create what is now known as the transistor name, being the one that stores the value of one of the two states that can occur. The combination of these logical states gives rise to logical operations, which are commonly known as gates (AND, OR, NOT, etc.) that what they do is decide what will happen in the output if there are specific conditions in the inputs. Besides, it must be mentioned that the combination of these bits also gives rise to words, numbers, or operations, conventionally grouping into 8-bit packages, calling this term byte. Playing with all this you can build powerful computers capable of deciphering almost any problem that arises. Needing to emphasize the word "almost" because it will play a fundamental role to understand the new era of computers that comes.

As anything that helps the human being to be more efficient, we try to squeeze as much as possible to give the maximum possible benefits to discover more and more. This has resulted in wanting to make more and more powerful devices by decreasing the size of these information transistors on a nanometric or even atomic scale, to fit inside chips. This is related to Moore's law states that approximately every two years the number of transistors in a microprocessor is doubled. This has reached such a point where the "classical" laws cease to make sense and become part of the mysterious world of the quantum, of quantum physics. These phenomena begin to occur when we work on a nanoscale, that is when we start to manipulate atoms.

E.3 Nanotechnology

The beginning of the era of nanotechnology possibly started thanks to one of the greatest scientists of all time, Richard Feynmann. In his famous talk of 1959 (there is plenty of room at the bottom), he introduced us that we could work with particles at the micro or nanoscale, this insignificant phenomenon possibly helped to make society think that there was greater potential in the microscopic world than had been assumed until then, both at the physico-chemical level and at the biological level.

The technological goal of this term refers to being able to manipulate atoms and molecules to subsequently produce products at that nanoscale (around 1 to 100 nm). Much research has been done in this field, from curing diseases through the famous drug delivery, nanomaterials to create more robust devices or regenerate tissues through biological nanoparticles.

And it is from this scale when we begin to have quantum phenomena that prevent us from moving forward, touching redefine the concept of logic and certainty, and beginning to talk about uncertainty and physical probabilities. Precisely, these phenomena are responsible for today is talking about quantum computers. Also predicted by Feynman in his famous talk of 1981, he proposed the use of quantum computers for the efficient simulation of quantum systems.

E.4 Introduction to Quantum Computers

The first quantum computer, it can be considered that it was created by the company DWave in 2007, and since then many companies have joined, the IBM company being the one that last January 2019, launched the first commercial quantum computer of 20 qubits.

As the reader can see, today, there are already the first replicas of what may be future quantum computers but what is and how these computers work or should work. First, a quantum computer does not work with transistors, that is, it does not work with devices that operate in only one state at a time, or on or off, or 0 or 1. On the contrary, these computers work by overlaying state.

This superposition of states can be explained by the Bloch sphere, alluding to the Swiss physicist Felix Bloch, which is a geometric representation of the pure state space of different quantum levels. The following figure E.1 show a Bloch sphere for two states.

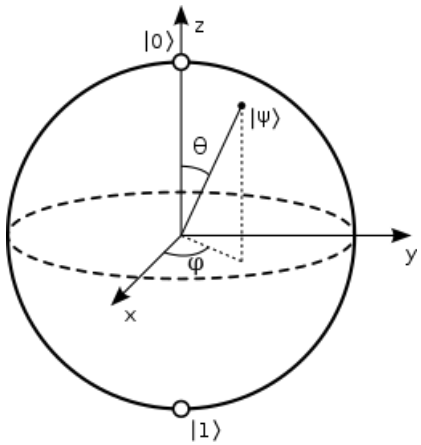

Figure E.1: Bloch sphere for two states, 0 and 1.

This sphere serves to represent any quantum state or qubit through the parameter $|\Psi$. Being able to express two states in the following way, where $0 \leq \theta \leq 2\pi$ and $0 \leq \phi \leq 2\pi$ are real numbers:

$$|\Psi = cos(\theta/2)\,|0> + e^{i\phi} sin(\theta/2)\,|1> \tag{E.1}$$

Also, this sphere serves as a visualizer of the action of different logical gates in quantum computing, or the temporal evolution of the state of a two-level system described by a Hamiltonian.

Assuming the case of two overlapping states, you could put the example of a coin-toss coin that is thrown into the air, this simulation could be compared to a classic computer when the coin falls to the ground, that is, when we observe the state of the coin is defined (face or cross) and could simulate the behavior of a quantum computer while the coin is in the air being in a superposition of two states at the same time (face and cross) since it has not been observed. Much more famous is the experiment of the Schrodinger cat, where a cat inside a box with a probability of 50% of having been exposed to a deadly substance, it would be considered that not observing its status, it would be alive and dead at the same weather. In equation E.2, the wave-function of the superposition of two states is shown, being α and β the complex amplitudes, fulfilling

the condition E.3, and being the square of these complex amplitudes the corresponding probabilities.

$$|\Psi = \alpha|0> + \beta|1> \tag{E.2}$$

$$\alpha\alpha^* + \beta\beta^* = 1 \tag{E.3}$$

Although the functioning of quantum computers seems a little paradoxical and unreal, what is intended is to take advantage of the uncertainty of the superposition of states to create more powerful computers. This could be verified by the rule that a quantum computer grows exponentially in the form L^N, where N is the number of quantum bits and L the number of states overlapped at the same time, also called qubits. On the contrary, a classic computer would grow linearly.

The states of quantum particles are obtained because in a classical process, for example, a state could be assumed when material leaves or does not pass electrical current, in a quantum process, the easiest way to understand it, is about how the particle rotates, known as spin, or also by the polarization of a photon among others. This gives rise to having infinite different states at the same time, and in the end reproducing an optimal result when observing them.

Another subject that has not been discussed but that will undoubtedly be fundamental for the optical communications of the future is quantum entanglement, which is an exchange of information, between particles, instantaneously, i.e. at infinite speed. This will result in more secure communications where a third party can not intercept or steal certain information, solving cryptography problems.

As an overview, what quantum computers try to solve concerning classical computers, is the famous tunnel effect, where the behavior of certain particles is not properly defined, such as electrons, being able to cross a barrier of potential without having these particles, enough energy to do it, and also using the shortest path to cross it. This, as it can be supposed, generates many undesired effects in the expected results, and hence the quantum attempt to solve this effect by simultaneously calculating states at the same time.

The next chapter is focused on the use of superconductors to avoid some unwanted effects on these quantum computers.

E.5 Superconductors

In the first place, superconductivity was discovered by the Dutch physicist Heike Kamerlingh Onnes on April 8, 1911, in Leiden. Superconductors possess certain intrinsic capacity at a certain temperature (critic temperature T_c) where there is no loss in the electricity that passes through them, being the null resistance that they offer to the passage of the current. This critic temperature, usually, in most materials is near absolute zero. Fulfilling:

$$T << Tc \tag{E.4}$$

This means that the current that passes through the superconductor persists without having a power supply. This characteristic of quantum mechanics occurs in various materials such as tin and aluminum, various metal alloys, and some strongly doped semiconductors, and it is one of the main causes why superconductors are good candidates for quantum computers. The bad thing is that it is needed a lot of requirements

that will be explained in the next chapter.

Several theories explain part of the functioning of superconductivity, since today despite the number of technological advances that there is not yet known to exact science because this phenomenon occurs. However, some theories explain some related effects.

First, in 1933, the Meissner effect was discovered by which a superconducting material, below Tc, repels the magnetic field inside, this being one of the effects that magnetic levitation explains. And it was not until 1935 that brothers Fritz and Heinz London proposed a phenomenological "adjustment" to Maxwell's constituent equations, the London equations, that described the two basic properties of superconductors: zero resistance and exclusion of the field (Meissner Effect).

London theory despite successfully describes several aspects of the electrodynamics of superconductivity can not determine the surface energy at the normal superconductivity phase interface. For this reason, in 1950 the Ginzburg-landau theory was enunciated, from which emerged two important parameters called the coherence length ξ and the penetration depth λ, which play an important role in characterizing what type of superconductor we have, through the parameter k:

$$\kappa = \frac{\lambda}{\xi} \tag{E.5}$$

Being:

$$\text{Type I} \longrightarrow \kappa < \frac{1}{\sqrt{2}}$$
$$\text{Type II} \longrightarrow \kappa > \frac{1}{\sqrt{2}}$$

It is important to note that in 1957 Alexei Abrikosov proved that a magnetic field penetrates in type II superconductor in the form of quantized vortex filaments (vortices) generating a mixed state. This theory gained importance after the discovery of superconducting materials of high temperatures (above 30 K) in 1986 since they produced this effect.

On the other hand, in 1957 the BCS theory was enunciated, in honor of Bardeen, Cooper, and Schrieffer, which explained, unlike GL theory, microscopic properties of superconductors. Cooper who took the first significant step when he showed that electrons could pair, by a weak interaction, at low temperatures, which has been called "Cooper pair". Behaving these electrons as bosons, and characterizing the "glue" that holds electron pairs together, by the vibrations of the ion lattice.

Another great effect that occurs in superconductors was discovered in 1962 by Brian David Josephson, which would not be confirmed until years later by Anderson and Rowell. This effect consists of two superconducting materials that produce the tunnel effect through a barrier of insulating potential (around 2-3 nm) [42, 6, 43]. This produces a supercurrent where the Cooper pairs can have a coherent behavior, where the wave behavior of these electrons is fundamental. This supercurrent can be expressed by the equation E.6.

$$I = I_0 sin\delta \tag{E.6}$$

Being I_0 the maximum supercurrent value and δ the phase difference between the two superconductor phases [43].

E.6 Requirements of Quantum computers

The requirements that a quantum computer must meet, are conventionally set by the famous DiVincenzo criteria proposed by the physicist David P. DiVincenzo in the year 2000. These criteria is a set of 7 rules, which are divided into two parts in the necessary conditions for quantum computing, which are a total of 5, and the necessary conditions to implement a quantum communication, being 2 conditions.

In the case of quantum computing the conditions are:

- The initialization of the state of the qubits to a well-known state. This is done by letting the system adapt to the ground state, which imposes restrictions on the speed of the operation.
- A scalable physical system with a well-characterized qubit, being a qubit a 2-level system with some energy gap. Also, the computer must be scalable by operating in the Hilbert space with a finite number of operations and must be correctable, being possible to extract the entropy of the system to maintain the state
- Long relevant decoherence times, being necessary that the decoherence times be large enough to not break the operating time. This property occurs because the particles are continuously changing state, and it is necessary to isolate the system sufficiently so that the particles can not interact with each other, otherwise the state would break.
- A "universal" set of quantum gates. Algorithms are restricted to the number of gates. However, the perfect implementation of gates is not always necessary.
- A qubit-specific measurement capability. If the measurements are non-destructive. Measurements that are not perfectly efficient are typically repeated to increase the success rate. A clear example can be detectors that have come to measure the number of photons that pass through a cross chapter.

And in the case of quantum communication the conditions are:

- The ability to interconvert stationary and flying qubits and the ability to faithfully transmit flying qubits between specified locations. Nowadays, for quantum communication, this chapter is essential since it is necessary to send the quantum keys to "decode" the information sent. The main problem that these qubits present is that most of them are stationary and can not be moved from the laboratory, and in addition to wanting to move one of the qubits to another place, the problem of decoherence in the photon is presented. It has to interact with the two qubits, for instance with other particles of the atmosphere.

The interferences that occur in these cases are called colloquially as noise, being the main problem of quantum computing. This as expected, gives us erroneous results. To avoid these problems, it is required to work in a vacuum and at very low temperatures, close to absolute zero, that is, to freeze the system, avoiding dissipations of heat or interactions with the environment among others.

The way to freeze certain materials is usually done through cryogenic liquids, which are obtained from liquefying the corresponding gases (Cryogenics) thanks to a technique developed by thermodynamics in the 19th century: the Joule-Thomson effect.

Being the liquefiers, machines that pump the heat out of the gas by subjecting it to a series of successive expansions and compressions.

Nowadays the best correction mechanisms, known as QEC (Quantum Error Corrections), are around 10^{-4}, getting in temperatures close to mK.

E.7 Resonators

The interaction of matter and light is one of the fundamental processes occurring in nature, and its most elementary form is realized when a single atom interacts with a single photon. Reaching this regime has been a major focus of research in atomic physics and quantum optics for several decades and has generated the field of cavity quantum electrodynamics. A lot of research has performed experiments in which a superconducting two-level system, playing the role of a qubit, is coupled to an on-chip cavity consisting of a superconducting transmission line resonator, showing that the strong coupling regime can be attained in a solid-state system, and observing the coherent interaction of a superconducting two-level system with a single microwave photon [6].

So conventionally, a resonator is a device that comes into resonance at certain frequencies, that is, the amplitude of the wave is greater at certain resonance frequencies, these frequencies being designed in the simulation of the device depending on different parameters such as height or thickness of the material among others.

Superconducting properties and CPW (Coplanar Waveguide) resonators offer several advantages for their application in circuit QED (Quantum Electrodynamics). On the other hand, CPWs can be easily designed to operate at specific frequencies, up to 10GHz or higher, and their impedance can be controlled at different lateral size scales. Their small lateral dimensions allow us to realize resonators with extremely large vacuum fields due to electromagnetic zero-point fluctuations, a key ingredient for realizing strong coupling between photons and qubits in the QED circuit. Moreover, CPW resonators with large internal quality factors of typically in the several hundred thousand ranges can be realized. Their resonant frequency is controlled by selecting the resonator length, i.e. in the few-millimeter order, and its loaded quality factor is controlled by its capacitive coupling with the input and output transmission lines (TL). This planar structure is patterned on a dielectric substrate, normally non-doped silicon (Si) or sapphire (Al_2O_3), and can be done by conventional photolithography methods, being commonly the superconducting materials aluminum (Al), which is the one that it will be used, and niobium (Nb). [23].

E.8 Quantum bits

Conventionally, the idea that comes to us when thinking about a qubit is the spin of an electron, where it can be positioned in an intermediate position between zero and one. And in the beginning, this was the first physical infrastructure that was created to give life to a qubit. This infrastructure is no longer used because spins are very sensitive and difficult to handle, however, they have very good properties such as a high time of overlap or compatibility with the manufacture of current chips.

As a second point, they have used and continue to use ion traps, which are characterized by an atom that is detached from an electron and acquires a positive charge. These ions through electric fields can be confined and through a series of lasers can interact with them to generate quantum operations, and are one of the most used in simulation issues, also stand out for their few defects and their great scalability, reaching to the date to generate more than 40 ions.

As a third point, we have also worked with photonic circuits, but due to their difficult handling due to the complexity of having control of the photons, since these do not interact with anything (a priori), they are being discontinued.

The last point, precisely what this work is based on, is superconducting circuits. These have the particularity that they are very easy to handle since basically the substrate in which conventionally works is usually silicon, this being a material, as is well known, with much work behind classic computers and therefore very scalable. As for disadvantages, it is a type of infrastructure that has short coherence times and in addition to the need, to date, to work at very low temperatures, bordering on absolute zero. But they are problems, that the big multinationals believe that it has an easy solution, that's why it is the best positioned nowadays to be part of the quantum computers of the future, and it is also the one that this project has been based on.

The chips based on the superconducting circuits are circuits that have a Josephson junction, previously explained in the chapter, by which they generate a supercurrent, simulating what we know today as qubits. As for the coherence times in the last 10 years, they have been improved by more than three orders of magnitude. In the following figure E.2 we can see a chip created by IBM company, through which these qubits are represented with their corresponding resonators.

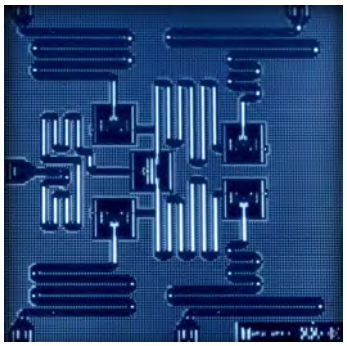

Figure E.2: An image of IBM's quantum processor showing five qubits with their respective resonators.

E.9 Present and applications

If before looking at the image of figure E.3, we had to imagine what a quantum computer would look like, we would probably try to reflect the aspect we have of the first classic computers. However, nothing further from reality occurs, since the number of restrictions that the latter impose, shows an aspect of the strangest for the reader who has not seen one.

Figure E.3: First classical computer from Apple company (left) vs first quantum computer from IBM company (right).

The approach that is currently being given to quantum computing is like a technology that will revolutionize the great advances of the future, but that there is still a long time for there to be a base solid enough for considerable efficiency. This is due to the number of drawbacks involved in working with such unstable systems that require insulation due to decoherence and temperatures close to absolute zero, among others.

The implications that this power of computing could give are unimaginable since it is thought that they could simulate millions of data to solve some of the problems that scientists of all disciplines have been looking for years, such as the famous problem of factorization (NP problem) used in classical cryptography, new nanomaterials, cures for many diseases, or with the help of quantum entanglement, make our communications "totally secure".

Additionally, these computers will be able to solve the problem of the many-body system that is when a node is added to a certain process and the execution time grows exponentially. And also, quite similar is the famous problem of the traveler that giving a certain number of points the processor must optimize which is the best route between the different points.

As the reader has been able to observe, nowadays it would not be possible to speak of quantum computers, if previously investigations in the field of superconductors or quantum physics, among others, had not existed. What we know is that companies like Google, IBM, Intel or DWave (in collaboration with NASA) are investing a lot of money in this sector that a priori aims to generate another technological revolution, or recently the news that the European Union has donated 1 billion euros for this field.

Even though the first commercial quantum computers are already arriving, as, last January 2019 IBM launched 20 qubits, there is still a long way to go. What is certain is that this technology will be linked to future superconducting materials and to the great research and discoveries in quantum physics that are intended to be made in the coming years. And although this technology may take 50 or 100 years, once this technology is established, the benefits it will provide will be gigantic due to its complete security thanks to the quantum entanglement and its exponential growth in processing capacity.

E.10 Timing of tasks (Gantt diagram)

This section visually (figure E.4) explains what has been previously described in methodologies. It must be remembered that this may vary due to the continuous problems that may arise when carrying out the work, since this will not begin until September 2019.

TASK NAME	START DATE	DUE DATE	DURATION	PHASE
Documentation (this report plus additional information)	sep.-19	jun.-20	287	Phase 1.1
Communication: continuos reporting and oral presentations	sep.-19	jun.-20	287	Phase 1.2
Reporting and writing	sep.-19	jun.-20	287	Phase 1.3
Writing of a possible article	mar.-20	may.-20	91	Phase 1.4
Design of 1st generation	oct.-19	dic.-19	60	Phase 2.1
Design of 2nd generation	dic.-19	feb.-20	61	Phase 2.2
Fabrication of 1st generation	dic.-19	feb.-20	61	Phase 2.3
Fabrication of 2nd generation	feb.-20	abr.-20	64	Phase 2.4
Fabrication techniques	sep.-19	oct.-19	29	Phase 3.1
Characterization techniques	oct.-19	oct.-19	13	Phase 3.2
Simulation techniques	sep.-19	sep.-19	28	Phase 3.3
Sonnet simulation	oct.-19	feb.-20	123	Phase 4.1
Electrical and physical characterization	abr.-20	may.-20	40	Phase 4.2

Figure E.4: Gantt diagram.

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