Physics BSc. Undergraduate Thesis

STUDY OF THE PENETRATION DEPTH IN THIN ALUMINIUM LAYERS

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Abstract

Superconducting electrical circuits can be used to implement a qubit (quantum bit), which is the basic unit of information in quantum computing. One of the main characteristics of superconducting qubits is their inductance, which is described by both a geometric and a kinetic term. Kinetic inductance is difficult to predict because it depends on the value of the penetration depth which, practically, depends on the thickness of the superconductor layer. Correlation between thickness and penetration depth has not yet been characterized for aluminium thin films, and would deviate considerably from bulk behaviour. In this project, the penetration depth value for aluminium thin films is determined using superconducting microwave resonators, which have been fabricated and tested experimentally. The fabrication process has been developed in order to maximize their efficiency. A relation between the penetration depth and the thickness has been obtained. For 200 nm Al thin film, the penetration depth value converges with the bulk aluminium value, i.e. providing a hint on threshold for type I superconductivity behaviour of bulk aluminium.

Contents

1 Introduction

Many problems that are considered unsolvable by classical computing are now being investigated in the context of quantum computing. Among the vast amount potential applications, there are some fields in which quantum computing could clearly have a great impact, such as encryption, quantum simulations and machine learning among others [1]. The distinguishing properties of quantum physics, such as superposition, coherence and entanglement, allow the processing information in radically different way with respect to classical methods. A qubit (quantum bit) is used as the basic unit of information instead of the conventional bit. The main difference between them is that the conventional bit can only have two values: 0 or 1, while the qubit can be in any superposition of these two states.

Several qubit implementations have been demonstrated for quantum computing such as using trapped ions [2], linear optics [3] and superconducting electrical circuits, among others. The last ones have several characteristics that are desirable when one wants to build a quantum computer. One of them is high circuit design flexibility. This means that the Hamiltonian of the system can be designed adjusting the parameters of the circuit. It is also easy to couple different qubits to each other and to measure and operate them using commercial microwave instrumentation. This scalability in terms of number of qubits and circuit complexity, also applied to fabrication methods, which can most rely on standard micro- and nanofabrication processes and methods from the semiconductor industry [4]. Other systems also have such characteristics, but superconducting circuits are showing great results [5].

The main component of superconducting qubits are the Josephson junctions. A Josephson junction consists in two superconducting layers separated by a thin dielectric material. Cooper pairs, which are pairs of electrons that move through the metal lattice without any resistance, can tunnel through the junction. Then, a supercurrent that flows continuously without any voltage applied is created. The other two important elements of such qubits are their capacitance and inductance. The last one is composed by a geometric and a kinetic term. The kinetic inductance is difficult to predict because it depends on the value of the penetration depth, which is related with the decay of the magnetic field that penetrates into a superconductor. The penetration depth depends on the thickness of the superconductor layer and it has not been characterized before for thin aluminium layers used to make superconducting qubit circuits. In order to improve the quality of fabricated superconducting qubits, a good prediction of the inductance's value is needed, which can only be achieved if an estimation of the penetration depth can be made.

Additionally, bulk aluminium and thin films behave differently. As will be detailed in the next chapter, thin-film aluminum may have undesirable properties that could affect the quality of qubits, such as the appearance of vortices. By contrast, bulk aluminum exhibits no such vortices. Therefore, it is important to understand the properties of thin-film aluminum and at what thickness it recovers the bulk properties.

2 Background

2.1 Superconductivity

Superconductivity is the property of certain materials to conduct direct current (DC) electricity without energy loss when they are cooled below a critical temperature (T_c). So, in the superconducting state, the material has zero DC resistance ($\sigma_{DC} \to \infty$). The supercurrent ($\vec{J}_s$) is carried by pairs of electrons, named Cooper pairs, which can move freely in the superconductor without being scattered. These paired electrons are held together by means of an exchange of virtual phonons. The distance between the two electrons that form a Cooper pair is the coherence length (ξ). Superconductors also expel the magnetic field, which is called the Meissner effect [6].

The London equations describe the relationship between the supercurrent and the electric ($\vec{E}$) and magnetic ($\vec{H}$) fields when the local limit can be applied [7].

$$\frac{\partial}{\partial t}\vec{J}_s = \frac{\vec{E}}{\mu_0 \lambda^2} \tag{1}$$

$$\nabla \times \vec{J}_s = -\frac{1}{\lambda^2}\vec{H}, \tag{2}$$

where λ is the London penetration depth. On the other hand, Pippard developed an empirical and more complex non-local equation for the supercurrent [8]. The difference between the local and non-local limit will be later discussed.

2.2 Penetration depth

The penetration depth is related with the decay of the magnetic field that penetrates into a superconductor. It can be derived from the London equations (1) and (2).

The explicit equation for the penetration depth at 0 K is [9]

$$\lambda_0 = \sqrt{\frac{m}{\mu_0 n e^2}}, \tag{3}$$

where m, n i e are the mass, density and charge of the Cooper pairs respectively, and μ_0 is the magnetic permeability in vacuum.

If the thickness of the material decreases, the penetration depth increases. To see this we must know that the coherence length (ξ) decreases when the electron mean free path (l_e) decreases. The electron mean free path is defined as the average distance over which an electron travels before substantially changing its direction or energy [6]. As l_e is limited by the thickness of the material, the coherence length decreases with decreasing thickness. And as $\lambda \propto \xi^{-1/2}$ [6] the penetration depth increases.

There is a relation between the penetration depth of aluminium and its normal resistance, which is the resistance that it would have the metal at 0 K. As in low enough temperatures aluminium is a superconductor because its critical temperature is $T_C \approx 1.2$ K [10], the resistance is usually measured at 4 K for convenience, where it is still a normal metal. When materials are in the local limit, there is an explicit equation for this relation. Later in this document, the local limit will be developed. The explicit formula that relates the penetration depth with the resistance in the local limit is [11]

$$\lambda_{\text{eff}} \approx 105\text{nm} \times \sqrt{\frac{\rho_N}{1\mu\Omega\text{cm}} \frac{1K}{T_c}}, \tag{4}$$

where T_c is the superconducting critical temperature. ρ_N is the resistivity, which follows from the formula

$$\rho_N = \frac{R\sigma}{l}, \tag{5}$$

where R is the resistance at 4 K and σ the transversal area. So $\sigma = td$ with d the thickness of the aluminium layer and t the lateral size of the squares that form the resonator's meander, which later will be introduced. In equation (5) l is the total length of the meander. So $l = tN$ with N the number of squares of the meander line. Then,

$$\rho_N = \frac{R\sigma}{l} = \frac{Rtd}{Nt} = \frac{Rd}{N}. \tag{6}$$

Finally, when the aluminium thickness is not much larger than the penetration depth, λ_{eff} is an effective penetration depth. So λ follows the equation [11]

$$\lambda = \sqrt{d\lambda_{\text{eff}}}. \tag{7}$$

2.3 Types of superconductors

There are mainly two types of superconductors according to the relation between the penetration depth and the coherence length. Type I superconductor has $\xi \gg \lambda$ (Pippard or non-local limit). Bulk aluminium is of type I. On the other hand, type II superconductors has $\xi \ll \lambda$ (London or local limit), and it is the case for thin aluminium films. In this regime vortices can be created. The presence of a vortex affects the coherence time of a qubit, which is related with how long a qubits retains a quantum state, i.e. information. Moreover, in this regime, a local form of Ohm's law can be applied and the London equations for superconductors are valid [6].

2.4 Kinetic inductance

A representation of a superconducting qubit with its three main elements is shown in Figure 1. It has a capacitance, a Josephson junction and an inductance. In this project we will study the inductance, which presents a geometric and a kinetic term.

In the expression of the energy associated with an electric current there is a term associated with the magnetic field that surrounds the current (geometric term). This magnetic field is generated by the self-geometric inductance of the wire carrying the current. There is another term in the energy expression due to the inertial mass of the particles that carry the electrical charge. In normal metals, this term can be neglected because it is proportional to the average scattering time of electrons, which even for the best conductors like copper is very short, thus leading to a small value of the kinetic energy. However, in superconductors it can have an important contribution because instead of electrons the current is carried by Cooper pairs which scatter elastically and thus experience no friction. This inertial mass is equivalent to an inductance, known as the kinetic inductance (L_k). Now, let us consider an homogeneous conductor with a uniform cross section and a uniform current density. Let us consider as well that the physical material properties of the conductor material like the permeability μ, the density n, mass m and charge e of the electron are independent of the magnetic field H and the current density J. Then, the formula of the total energy is [12]

$$E = \frac{1}{2}L_g I^2 + \frac{1}{2}\frac{ml}{ne^2\sigma}I^2, \tag{8}$$

where l is the length of the conductor, σ the area of the cross section and m, n and v are the mass, number density and velocity of the particles that carry the electric current. So, L_g is the geometric inductance. By analogy to L_g, the kinetic inductance is

$$L_k = \frac{ml}{ne^2\sigma} = \frac{\mu_0\lambda_0^2 l}{n\sigma}, \tag{9}$$

where in the last equality we used equation (3). It is clear that there is a relation between the kinetic inductance and the penetration depth.

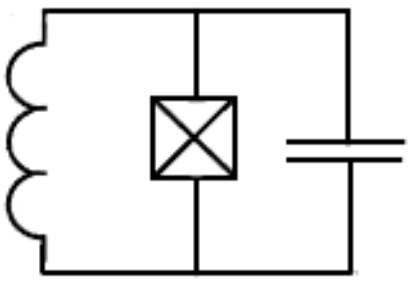

Figure 1: Representation of a qubit equivalent circuit composed of, from left to right, an inductance, a Josephson junction and a capacitance connected in parallel.

2.5 Superconducting microwave resonators

Superconducting microwave resonators are an important element in superconducting qubit circuits. They are used for qubit protection, to read out the qubit state, to couple different qubits and as a possible quantum memory [13]. Microwave resonators are electronic devices that act as electromagnetic wave oscillating systems. They present a resonant response at some specific frequencies, which are called resonance frequencies. They are mainly described by an inductive component and a capacitor element. Then, the energy stored in the resonator oscillates between the capacitance C and the inductance L with a frequency

$$f_r = \frac{1}{2\pi\sqrt{LC}}, \tag{10}$$

neglecting any external coupling and internal dissipation. The frequency of resonance for microwave resonators is in the microwave regime ($\sim 10^9$ Hz).

The penetration depth of the material can be obtained from the resonance frequency of a resonator (f_r) fabricated with such material. We know that the inductance has a kinetic (L_k) and geometric (L_g) term. We can express the resonance frequency as

$$f_r = \frac{1}{\sqrt{(L_g + L_k)C}}. \tag{11}$$

If f_r, L_g and C are known, L_k can be calculated. And the relation between the penetration depth and L_k is [9]

$$\lambda = \frac{L_k}{N\mu_o}, \tag{12}$$

where N is the number of squares of the resonator obtained.

The quality factor is an important characteristic of resonators. It is defined by the ratio of the energy stored in the resonator to the average energy loss per cycle times 2π. This value is related to the sharpness of the resonance frequency peak: the sharper, the higher the quality factor. If the resonator is coupled to a transmission line, which transmits the microwave signal, there are different contributions to the total quality factor. The internal quality factor accounts for the losses related with the resonator's material (Q_i). There is also an external quality factor that accounts for the coupling to the transmission line (Q_c). The total or loaded quality factor (Q_l) accounts for the internal losses and coupling losses. They are related by the expression

$$\frac{1}{Q_l} = \frac{1}{Q_i} + \frac{1}{Re\{Q_c\}}. \tag{13}$$

In the expression above there is only the real part of Q_c because the external quality factor also models the impedance mismatches which are absorbed in its phase.

3 Objectives

The main goals were:

- Measure the penetration depth for thin aluminium films.
- Determine at what thickness aluminium is a type I superconductor.

These objectives would allow to more accurately design qubit circuits and differentiate between the two types of superconductor behavior exhibited by aluminum.

The approach of this research project was first, designing, and second, fabricating aluminium microwave resonators. Then, extracting the inductance value without the kinetic term using a Sonnet simulation [14]. After that, measuring the resonators and assuming that all the difference between the inductance measured and the simulated value was due to the kinetic inductance. Finally, finding the penetration depth's value for each thickness, in particular in the thickness range from 25 nm to 200 nm. Furthermore, performing 4-probe measurements and using the relations explained in section 2.3 to find the penetration depth through the resistance of the material at 4 K.

4 Methodology

In order to experimentally determine the penetration depth, four main steps needed to be followed. The set of devices had to be designed, fabricated and, finally, tested. Then, the data obtained had to be processed and analyzed to provide meaningful results and allow discussion.

4.1 Design

My project supervisor David López had designed the samples with Python. In Figure 2a a single chip is seen with its four parts. Each part has a different type of resonators: small, medium, large and distributed. Different types of resonators are needed in order to have different kinetic contributions in the inductance. For example, for the smallest thicknesses wider resonators must be used in order to see

the kinetic contribution. The large, medium and small resonators are lumped LC resonators. In Figure 2b one of the parts that compose the chip can be seen with ten resonators joined by a feed line. There is also a launcher in the end of each line, a meander with four lines and three probing structures. Each resonator has a different length of the last three fingers in order to have a different value of the capacity but the same kinetic inductance. Then, there is a shift in the frequency between resonators of the same type. The ones with meanders have 15 meanders and 9, 17 and 36 fingers for large, medium and small resonators, respectively. The dimensions of each structure are in Table 4 in the Annexes section. The layout used had seven chips printed.

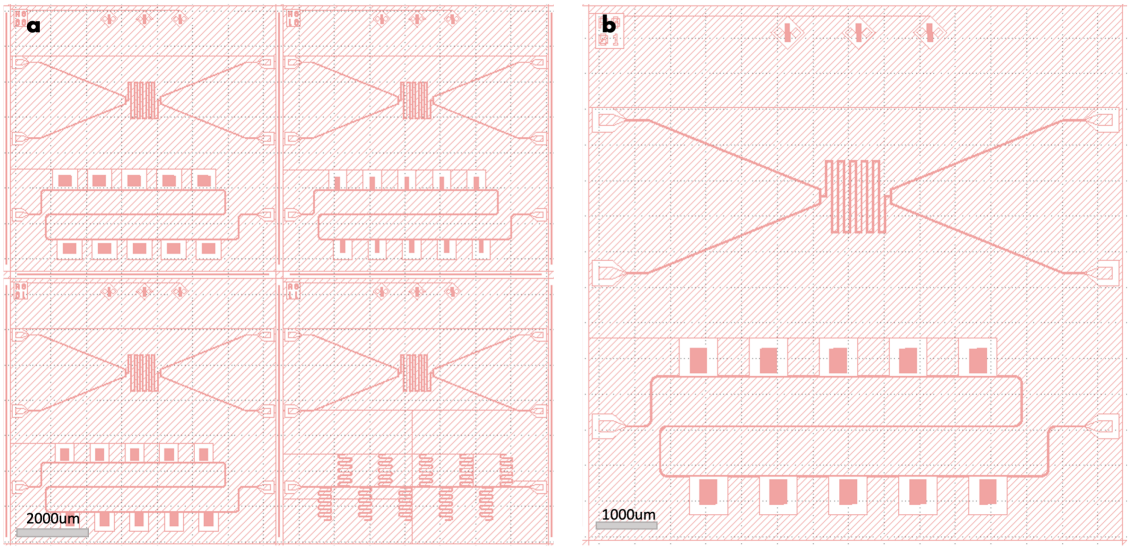

Figure 2: **a.** Design of a single chip. Top left: large resonators. Top right: small resonators. Bottom left: medium resonators. Bottom right: distributed resonators. **b.** Design of the medium resonators and the structure for the DC measurements.

Lumped resonators are two-port devices. For this kind of samples the signal transmission in the microwave regime is investigated. The resonators are lumped LC-type, the equivalent circuit and the actual circuit from one of the devices are shown in Figure 3a and 3b. Each resonator has an inductance, that is a meander, in parallel with a finger capacitance. Both are coupled to the feed line by a mutual inductance.

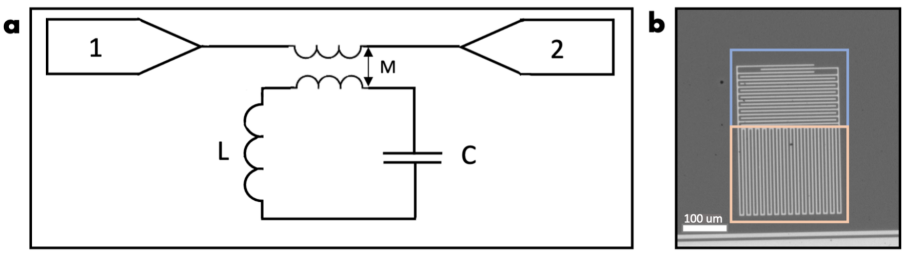

Figure 3: **a.** Equivalent circuit of a two-port sample. The resonator is represented as a capacitance and inductance in parallel, inductively coupled to a feed line. **b.** A medium resonator from the test22 sample characterized in the Table 6 in the Annexes section. The capacitance is the finger inside the blue square and the inductance is the meander inside the orange square.

4.2 Fabrication

Aluminum was used as the superconducting material. Conveniently, it presents good adherence over silicon wafers. Bulk Al has a superconducting critical temperature of $T_c \approx 1.2$ K [10]. This temperature

is easily achieved in a cryogenic dilution refrigerator. The whole fabrication process for implementing resonators testing at cryogenic temperatures consists in:

- Photolithography.
- Aluminium evaporation and resist lift-off.
- Chip dicing and devices wire bonding.

The aluminum is deposited on a substrate, which is a small part diced from a 4-inch high resistance silicon wafer. Silicon presents good properties when combined with superconducting resonators, such as low dielectric loss. Before starting with the photolithography, some optical resist was applied onto the silicon wafer in order to cut the wafer into 2 cm $\times$ 2 cm dice. Chip dicing was done by automated diamond saw cutting, and allowed to fabricate individual samples instead of at wafer scale, which was needed in order to produce devices with different aluminum thickness. Each chip was cleaned with two baths of acetone, one bath of isopropanol and nitrogen gas to dry, to remove the resist used to protect the silicon surface from potential scratches caused by dicing.

4.2.1 Photolithography

Photolithography is the process of transferring geometric features by selective light exposure of a thin resist layer with a mask, as schematized in Figure 4a. Photolitography consists in a step sequence, such as: thin film photoresist deposition, mask alignment and light exposure, and resist development. Before resist deposition a primer, Hexamethyldisilazane (HMDS), is applied to increase the adhesion of the photoresist on the silicon chip surface. Then, the photoresist is deposited by spin coating technique. We used a positive photoresist, which becomes soluble in a solvent once exposed to light. A photoresist is a material sensitive to light, typically a polymer, which includes an inhibitor and a solvent. After spin coating, a soft bake is applied to evaporate part of the solvent and solidify the photoresist thin film. When the polymer is exposed to radiation, changes its structure [15]. In the case of a positive tone, it reacts to light such as it becomes soluble in a suitable developer solution. The exposure step consists in applying a given amount of photons in the UV frequency regime through the mask that has been aligned over the chip. The pattern over the glass mask substrate is made with chrome. The chromium thin film does not allow the UV light to pass. The areas of the photoresist that get exposed to the right dose become more soluble when put on a certain solvent. This last step is the so-called development.

All the photolithography processes were done at the Integrated Micro and Nanofabrication Clean Room of IMB-CNM (Institut de Microelectrònica de Barcelona) [16]. The procedure and processing conditions for standard positive photoresist are the following:

- Dehydration. Place the chip at 120 $^{\text{o}}$C in an oven for 10 minutes to take out any moisture that may remain on the chip surface.
- Primer deposition. Put the chip in the Delta 150 equipment to apply Hexamethyldisilazane (HMDS).
- Photorest deposition. Pour photoresist HIPR6512 by spin coating technique. This produces a thin uniform layer of photoresist on the surface. In this case 1.7 μm thick resist layer was used.
- Soft bake. Place the sample at 80 $^{\text{o}}$C on a hot plate for 2.5 minutes to harden the photoresist.
- Place the mask in a Karl Süss MA6 aligner.
- Alignment. Introduce the chip and center it with the mask structures that should be patterned. Make the exposure for 13.5 seconds with a gap of 50 μm or hard contact and a wavelength of 365 nm.
- Post exposure soft bake. Place the sample at 80 $^{\text{o}}$C for 2 minutes and wait 1 minute to cool down. This bake reduces a phenomena caused by the destructive and constructive interference patterns of the incident light: the standing wave phenomena [17].
- Development. Immerse the chip in OPD 4262, which is the developer, for 35 seconds and, then, rinse twice in deionized water for 30 seconds each.

- Blow dry with nitrogen gas.
- Soft bake. Place the sample at 115 ^{o}C for 5 minutes. This step hardens the photoresist and improves its adhesion to the chip surface.

In some chips, LOR3A was added before applying the HIPR6512. With this two resists (LOR3A and the standard resist) there is better resist profile in preparation for pattern transfer by metal deposition and resist lift-off approach [18]. LOR3A, has higher sensitivity and therefore certain undercut is obtained. This undercut facilitates the lift-off easing the resist solvent to access the resist underneath the evaporated metal thin film. The LOR3A requires a soft bake at 90^{o}C for 5 minutes.

4.2.2 Aluminium evaporation and resist lift-off

Aluminium was deposited over some chips in the Plassys MEB550S placed in IFAE's (Institut de Física d'Altes Energies) clean room. The recipe used is specified in Figure 13 in the Annexes section. The thickness of the aluminium deposition is the only parameter changed between the different chips. To compare fabrication yield and materials characteristics, some of the aluminum evaporations were also performed in the LEYBOLD UNIVEX 400 at the Integrated Micro and Nanofabrication Clean Room of IMB-CNM [16]. Similar to photolithography this process was done by the respective processing area engineer following a standardized procedure.

The resist lift-off after the metal deposition on the patterned resist, completes the pattern transfer, in which the aluminum in direct contact with the silicon substrate remains, but not the aluminum on top of the resist. In Figure 4b there is a scheme of both processes: the evaporation and the lift-off.

In some cases, the lift-off was done at IFAE's clean room. The procedure steps were:

- Pour 175 ml of NMP (n-methyl-2-pyrrolidone) in a beaker and place it over an electric hot plate with a magnet and a thermometer inside.
- Increase slowly the temperature of the hot plate in order to reach 80 ^{o}C.
- Introduce the chip inside the recipient and at 600 rpm, so a magnet stirs the NMP.
- Squirt the chip with a pipette to help the extra aluminium leave and wait for an hour and a half.
- Stop the stove and put the chip in IPA (isopropanol).
- Dry the chip with nitrogen gas.

When the lift-off was done at IMB-CNM's clean room, the following procedure was applied:

- Immersion of the sample in acetone for 5-10 minutes.
- Apply short ultrasonication treatment.
- Rinse in IPA.
- Blow dry in N_2.

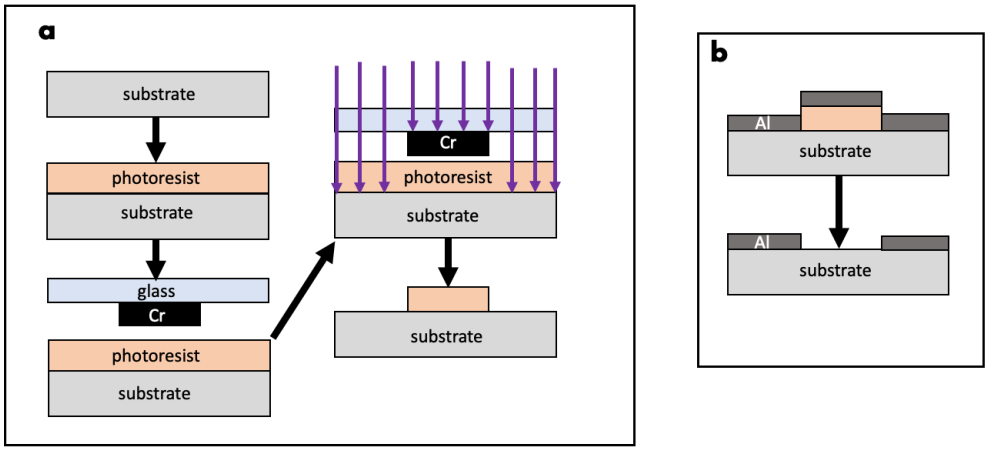

Figure 4: Steps of the fabrication. **a.** The photolithography main steps. Photoresist application, mask alignment, exposure and development. **b.** The aluminium evaporation and lift-off.

4.2.3 Dicing and wire bonding

The sample dicing before encapsulation for cryogenic electrical characterization was also done by IMB-CNM ICTS staff. Each chip was diced in four smaller squares corresponding to the areas described in Figure 2a.

The wire bonding was used to electrically connect the sample devices and structures to a PCB, as shown in Figure5b. Wires are depicted as black lines in Figure 5a and were made of aluminum. For each chip, 94 aluminium wires should be placed, but this was difficult to achieve because of the presence of contaminants on the samples, which may lead to a non-sticking surface, among other issues. The AC lines and the ground near these lines should have more cables in order to reduce the impedance of the connections. The wire bonding could be done both at IFAE or in IMB-CNM with a special-purpose wire-bonding machine, which could be operated in either automatic or manual mode.

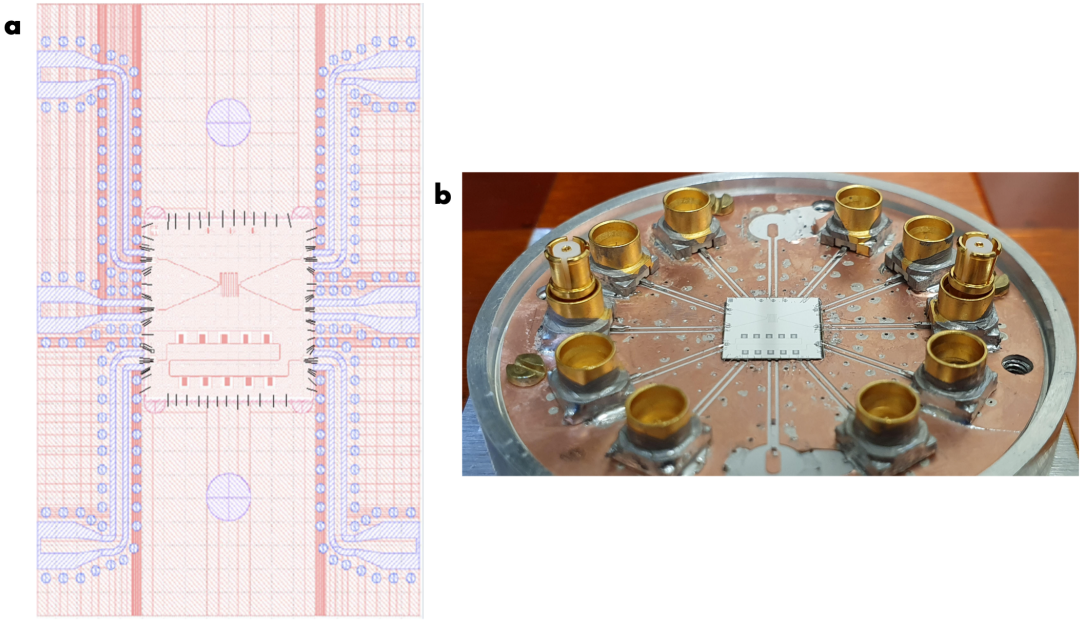

Figure 5: Wire bonding **a.** Desired distribution of the wires between the device's pads and grounding and the PCB lines. **b.** Device wire bonded to a PCB.

4.3 Measurement

Aluminium has a superconducting critical temperature of $T_c \approx 1.2$ K [10]. Thus, the samples needed to be cooled below 1.2 K to exhibit superconductivity. Also, for small temperatures the quality factor is big enough to be seen. To achieve such temperatures we used a refrigerator that gets below 20 mK. The model used was a cryogen-free dilution refrigerator from BlueFors [19]. To reach such temperatures first it creates the vacuum. Then, it gets to 4 K using a pulse-tube compressor with 4-He gas. And finally reaches mK mixing the two isotopes of helium, 3-He and 4-He.

The setup for the measurements is shown in Figure 6. There are different stages, each one at a different temperature. There is also 50 dB attenuation in the input signal. For the output there is 40 dB amplification after an attenuation that avoids the creation of a stationary wave. The attenuation helps to reduce the thermal noise in the signal. Outside the refrigerator there is 60 dB more amplification. The signal generation and the measurement is performed by a vector network analyser (VNA). For the 4-probe measurement the signal goes through the DC cables, so there are two inputs and two outputs. In order to measure different samples in one run of the refrigerator a switch is placed inside the cryostat.

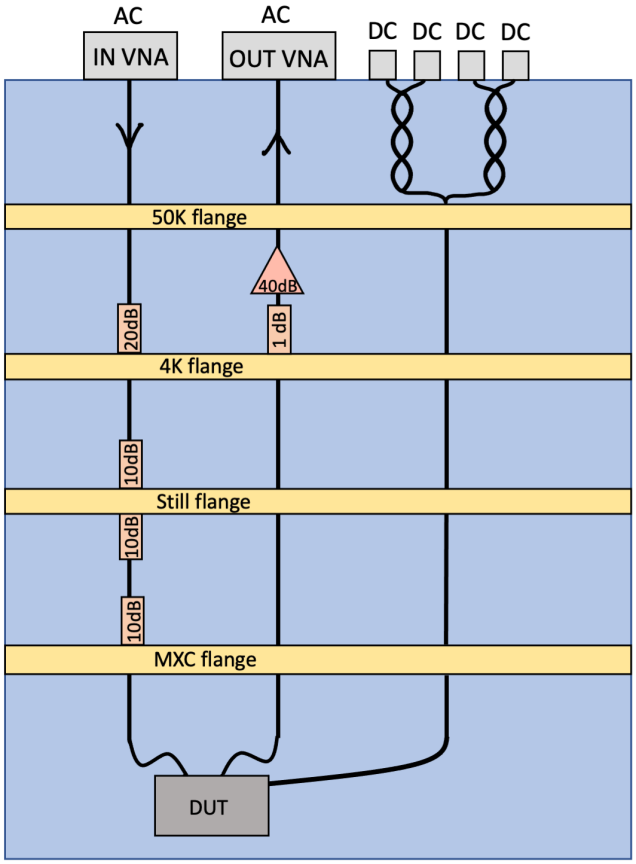

Figure 6: Diagram of the refrigerator's setup. There is an input channel that goes from the VNA to the sample and has 50 dB attenuation. There is also an output channel that comes from the sample to the VNA with 40 dB amplification. The DC cables are used for the 4-probe measurement.

4.4 Analysis

4.4.1 Resonators measurement

For each resonator on each chip we obtained the transmission S21 in dB depending on the frequency of the microwave probe signal. The input signal reaches the chip and is partialy reflected and partialy transmitted. We used the Labber software from Keysight to obtain the values of the transmission coefficient acquired by the VNA. For each resonator, the expected result of the absolute value of the transmission is a Lorentzian function centered at the frequency of resonance of the resonator. That is

not always true as sometimes the environment moves it away from the ideal behaviour. This is due to the possible cable losses and amplification, the length of the cables and the finite speed of light. Figure 9 shows two resonance responses. In Figure 9a the shape seems a Lorentzian but in Figure 9b it is far from the expected result. Therefore, instead of fitting a Lorentzian to find the values needed, the fitting was made following the procedure and Python code from [20]. It uses an algebraic method that does not rely on optimizers. So, it does not need initial parameters. It fits the function

$$S21(f) = ae^{i\alpha}e^{-2\pi i f\tau}\left[1 - \frac{(Q_l/|Q_c|)\,|e^{i\phi}}{1 + 2iQ_l\,(f/f_r - 1)}\right], \tag{14}$$

where the environmental term is $ae^{i\alpha}e^{-2\pi i f\tau}$. The constant a is an additional amplitude, α counts for the possible phase shift, and τ for the electrical delay. The algebraic method first finds the constants a, α and τ. Then, looks for the internal quality factor (Q_i), the total quality factor (Q_l), the module of the external quality factor ($|Q_c|$), its corresponding phase (ϕ), the resonance frequency f_r, and the error associated to each parameter. The values of L_g and C are needed to find L_k as has been explained in section 2.4 using the simulator Sonnet. With the pictures of the structures measured obtained by a scanning electron microscope (SEM), the actual sizes of the resonators were found. These values were used in the Sonnet simulator to obtain the resonance frequency without taking into account the kinetic inductance. The values of L_g and C could be extracted in this way. Once L_g and C were determined, the kinetic inductance could be found with equation (11). Then, the number of squares N was also found with the SEM images. With N and L_k the penetration depth was finally calculated with the equation (12).

4.4.2 Resistance measurement

4-probe measurements were performed to avoid the possible contact resistance between the probe and the sample. Current went through the two outer probes and the voltage across the two inner probes was read. Then, changing the value of the current, data with the current and the voltage at 4 K was obtained. Doing the corresponding linear regression we got the resistance (R). With the SEM images of the samples the number of squares of the meander N could be found. The critical temperature could be obtained changing slowly the temperature of the refrigerator and seeing when the device stopped acting as a superconductor. A current of 0.5 μA was applied and the voltage was measured. The temperature of the refrigerator was slowly increased. When the voltage stopped being constant it meant that T_c was reached.

The electron mean free path (l_e) depends on the aluminium thickness. We used thin layers of this material. So, l_e in our device is short compared with the penetration depth. Therefore, we were in the local limit, where the formulas explained in section 2.2 could be applied. With all the values and the equations (4), (5), (6) and (7) the penetration depth was found.

5 Results

5.1 Fabrication

Table 5 in the Annexes section compiles the fabrication processing of the set of samples produced and tested in this study, specifying when and where was the photolithography, the evaporation and the lift-off performed for each chip fabricated. Also, whether LOR3A was applied and the aluminium thickness. We fabricated 27 chips with aluminium thicknesses between 25 and 200 nm. Based on optical microscope inspection, the devices to be electrically tested were selected. The chosen ones were diced and wire bonded. The evaluation of the fabrication of each chip after the lift-off is compiled in Table 6 in the Annexes section.

Fabrication yield can only be assessed upon resist lift-off, as only after this step some photolithography and metal deposition related issues, as well as lift-off constraints, are revealed. In Figure 7a the difference between obtaining a good versus a bad lift-off result is shown. We saw that performing the lift-off by IMB-CNM procedure we obtained better results than in the IFAE clean room. Then, we decided to follow the second protocol explained in 4.2.2. Figure 8c shows the yield for the lift-off performed in IMB-CNM and at IFAE. The ones at IFAE were also evaporated there, with a thickness of 100 nm and without LOR3A. As can be seen, in IMB-CNM the results were better in general. We only did three chips in total with the lift-off at IFAE. In Figure 8d the yield is shown depending on the aluminium

thickness which for 200 nm it is very low. That is because for large aluminium thicknesses the lift-off can be more easily compromised depending on resist profile as shows Figure 4b.

Most critical structures fabrication have been the small resonators, with only a yield bigger than zero for 50 nm and 100 nm thicknesses. This was due to the uncertainty of the photolithography process, which accounts for the lateral uncertainty and the possible interference that difficult the resist profiling. The small resonators have a meander and finger width of 2 μm, which is very close to the uncertainty of the photolithography process. So, it is very hard to achieve this kind of precision and the pattering usually is not correctly transferred. In Figure 7b the difference between two of the small resonators is shown, with bad photolithography on the left and good photolithography on the right. In Figure 8d the total yield depending on the thickness is shown which, for small resonators, the yield is very low and somehow random. To overcome this limitation another lithography method would be needed. Electron beam lithography, in which instead of light a very fine electron beam is used to locally modify the thin film resist chemically, could be a most convenient option, based on a resolution or accuracy in the nanometer order.

Furthermore, in the photolithography there was a problem with the mask cleaning. After each photolithography the mask should be cleaned as pieces of photoresist can remain there. We tried to clean it with acetone and IPA but it did not work. Usually, they are cleaned with piranha[1], with the OBDUCAT QS W 300SM machine placed at the Integrated Micro and Nanofabrication Clean Room of IMB-CNM [16]. The glass mask used was too thin, i.e. fragile, to apply effective cleaning methods. The consequences of the remaining pieces of solid photoresist can be seen in Figure 7c.

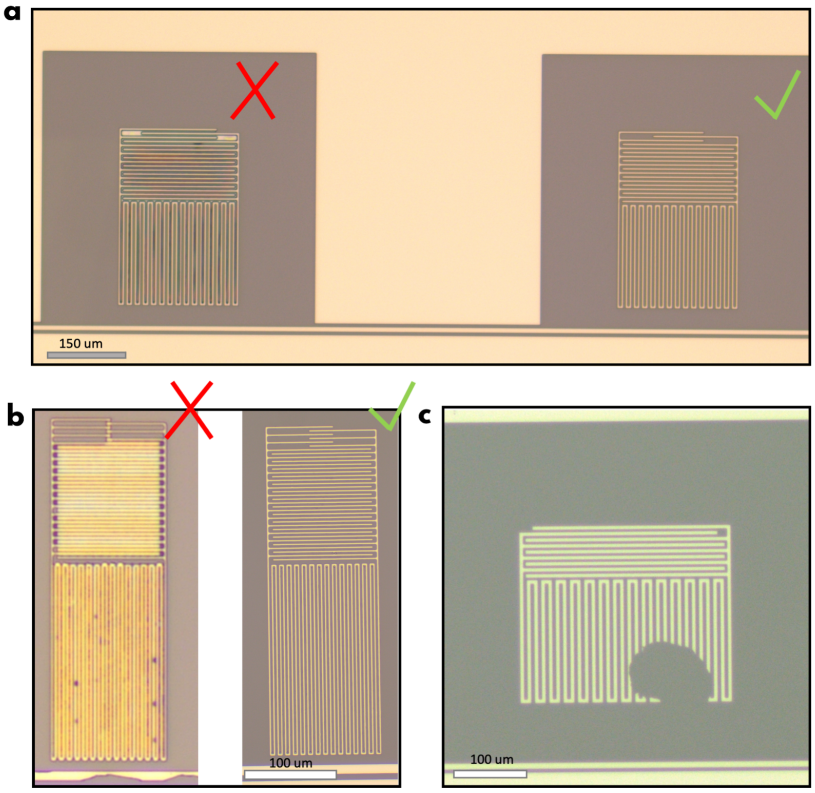

Figure 7: Images of different resonator structures made with an optical microscope in IFAE, after the lift-off procedure. **a.** Two medium resonators from test07, with an aluminium thickness of 100 nm and the lift-off done at IFAE. The left one had a bad lift-off while the right one had a good lift-off. **b.** Two small resonators both of them with an aluminium thickness of 100 nm and without LOR3A. The left one from test02 shows a bad photolithography. The right one from test01 shows a good fabrication process. **c.** A large resonator from test10 with a defect due to limitations in the cleaning of the photolithography mask.

[1]Piranha solution is a mixture of sulfuric acid and hydrogen peroxide used to remove organic residues from substrates.

Due to the very thin films used and the softness of Al, another difficulty was not to scratch the chip in none of the steps or manipulation of the samples. Scratching happened especially during the chip dicing or the wire bonding.

Some of the pictures of the structures done by a scanning electron microscope (SEM) are in Figure 15a and 15b in the Annexes section. The actual sizes of the resonators were extracted from them and are in the Table 4 in the Annexes section. The dimensions differ from the nominal design values due to the limitations of resolution in the fabrication processes.

In Figure 8a fabrication yield as a function on whether the Al evaporation was done at IFAE or IMB-CNM is shown. Although we evaporated only seven chips at the IMB-CNM, the yield is higher than IFAE's. The lift-off procedure followed at the IMB-CNM clean room presents better results, as Figure 8c shows, which indicates that using acetone and ultrasonication treatment is more efficient. A proper comparison would require set of samples in which all the combination for evaporation as well as lift-off, done at IFAE or IMB, and LOR3A application can be performed. Also, in Figure 8b we see that using LOR3A the large, medium and distributed resonators yield is better. But for the small resonators the yield is worse. So, in general, it can be stated that using LOR3A fabrication results are partially better. As shown in Figure 8d, the worse yield is obtained for a thickness of 200 nm as the lift-off is harder. For thicker resonators, 200 nm and above, a different technique could be tried like magnetron sputtering. The best yield is for 50 nm except for the small resonators showing the best yield for 100 nm. In general, the medium resonators are the easiest to fabricate. Finally, a new mask should be fabricated in order to achieve better results. One that can be thoroughly cleaned.

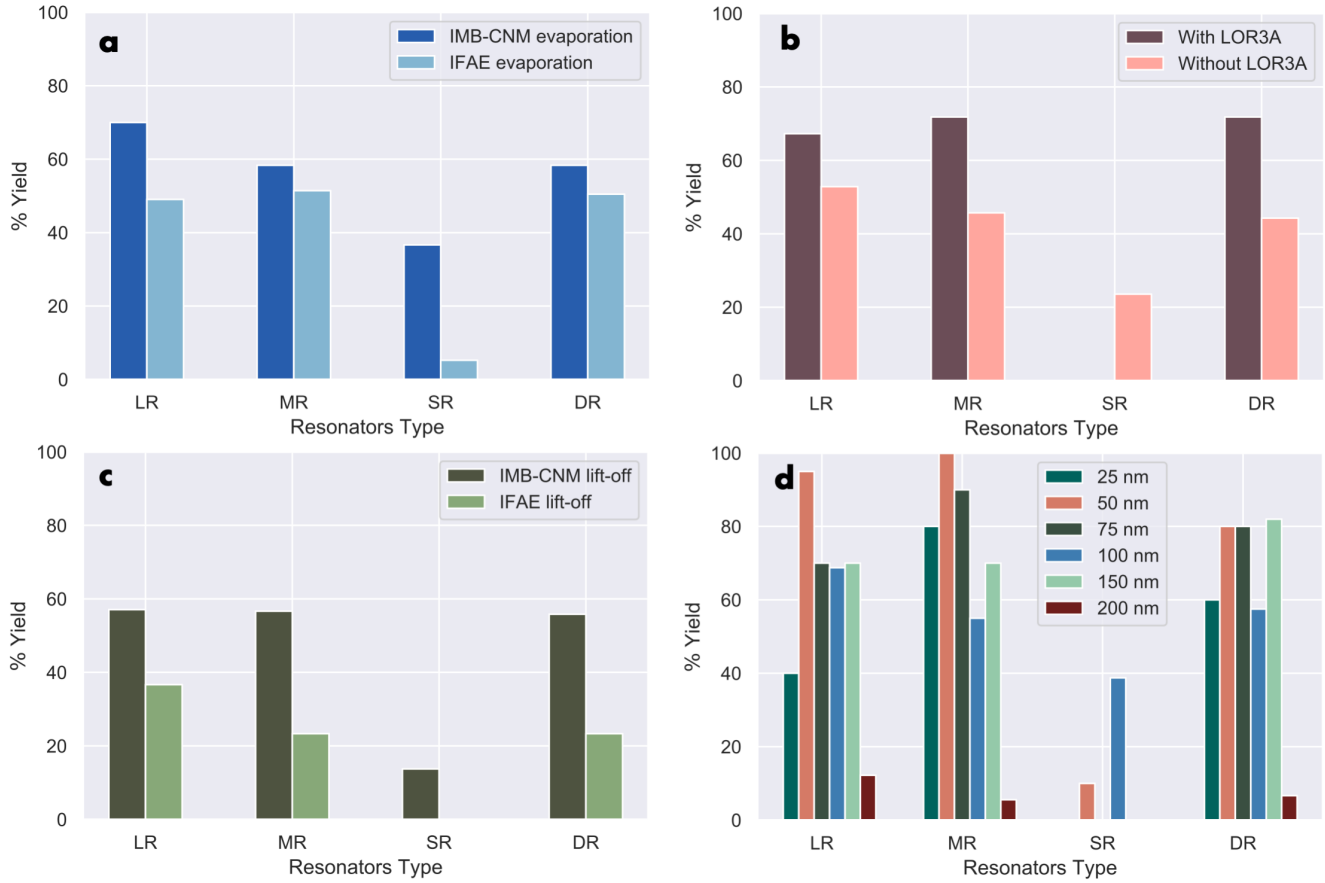

Figure 8: Yield of the fabrication. **a.** Yield depending on the place of the aluminium evaporation. **b.** Yield depending on the application or not of LOR3A. **c.** Yield depending on the lift-off's place. **d.** Yield as a function of aluminium film thickness.

5.2 Device measurements

In Table 1 the main characteristics of the five chips measured are shown. As can be seen, for two of them the 4-probe measurement could not be performed because the lines of the wire bonding were damaged during the cool down. Moreover, there is a difference between the number of resonators seen and the ones that were actually fitted. This happened because in some cases the shape of the transmission function depending on the frequency was too diverted from the expected one to be fitted. So, in these cases, the resonators were not used to calculate the penetration depth.

Chip	Nominal aluminium thickness (nm)	Type	4-probe	Resonators seen	Resonators fitted
test22	25	MR	Yes	9	7
test10	50	MR	No	10	10
test20	75	LR	No	9	8
test06	100	SR	Yes	10	9
test24	200	MR	Yes	6	0

Table 1: Measurements main characteristics.

5.2.1 Resonators measurement

We measured each chip at different temperatures, from $T \approx 20$ mK to $T \approx 700$ mK. We used a wide range of temperatures because there is also a relation between the penetration depth and the temperature [21], so in the future this could be studied. After the measurement, we fitted every resonator. In Figure 9a and 9b there are two examples of the fitting. As can be observed, the method used not only fits well the data with a Lorentzian shape, also the ones with a more complicated shape. There were some difficulties with the fitting as in some cases two resonant frequencies of two different resonators were too close. In this case only one could be fitted. Furthermore, some of them followed a more complicated shape, so they could not be fitted. Although in general the results were good.

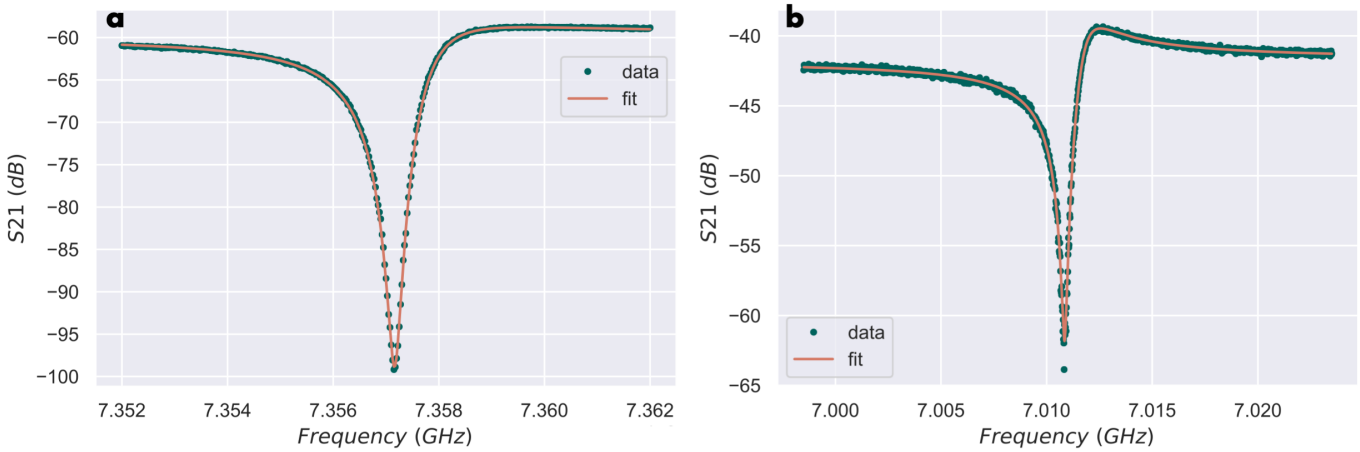

Figure 9: Data and fit results for two different resonators. **a.** Transmission depending on the frequency for the fourth resonator of the test20 measured at 33 mK. **b.** Transmission depending on the frequency for the first resonator of the test24 measured at 22 mK.

The values of the expected resonant frequency, L_g and C for each chip are displayed in Table 7 in the Annexes section. In Figure 10 there is an example of a Sonnet simulation, which was implemented using the dimensions from the pictures done by a scanning electron microscope (SEM) that are in the Table 4 in the Annexes section. The real dimensions differ from the nominal values, although this did not affect the results as the simulation used these dimensions. The Sonnet simulation shows the expected shape of the transmission depending on the frequency.

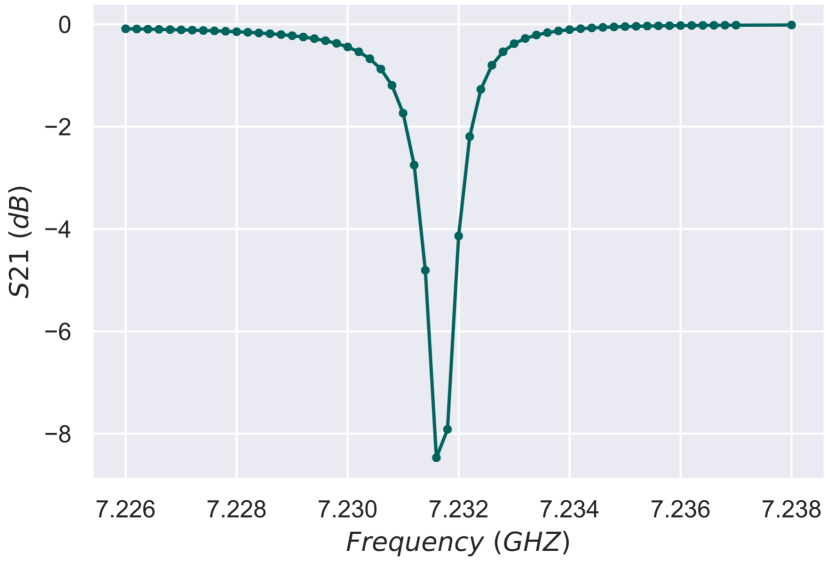

Figure 10: Transmission depending on the frequency for a medium resonator from a Sonnet simulation.

In Table 2 one can see the values of aluminium thickness and the corresponding penetration depth for the smallest temperature. We used data at this temperature because in this case nearly all the quasi-particles are paired up. To calculate the penetration depth we took the mean of the penetration depth of each chip's resonator. All the values are shown in Table 7 in the Annexes section. As can be seen, the penetration depth decreases when the aluminium thickness increases, which was what we expected.

Nominal aluminium thickness (nm)	Penetration depth (nm)
25	140.52±0.42
50	103.89±0.27
75	76.0±2.2
100	64.9±2.5

Table 2: Values of the penetration depth as a function of the aluminium thickness obtained from the measurement of the resonators.

5.2.2 Resistance measurement

We also performed 4-probe measurements for three tests. We found the resistance as the slope of the intensity applied versus the voltage measured. In Figure 11 there is a graph with the voltage depending on the current for test22 with its fitting, which had a correlation coefficient of $r^2 = 0.999$. Then, to find the value N of equation (6) we used the SEM images from the tests measured. The value found was $N = 1133.16$. Finally, the values of the critical temperature were determined. In Table 3 there are the values of the resistance, the critical temperature and the penetration depth found for each aluminium thickness.

Nominal aluminium thickness (nm)	Resistance (Ω)	T_c (K)	Penetration depth (nm)
25	1252.597±0.007	1.32±0.02	151.9±1.2
100	40.6598±0.0001	1.183±0.005	57.86±0.12
200	16.4749±0.0001	1.183±0.005	52.10±0.11

Table 3: Values of the resistance, the critical temperature and the penetration depth as a function of the aluminium thickness for the resistance measurement.

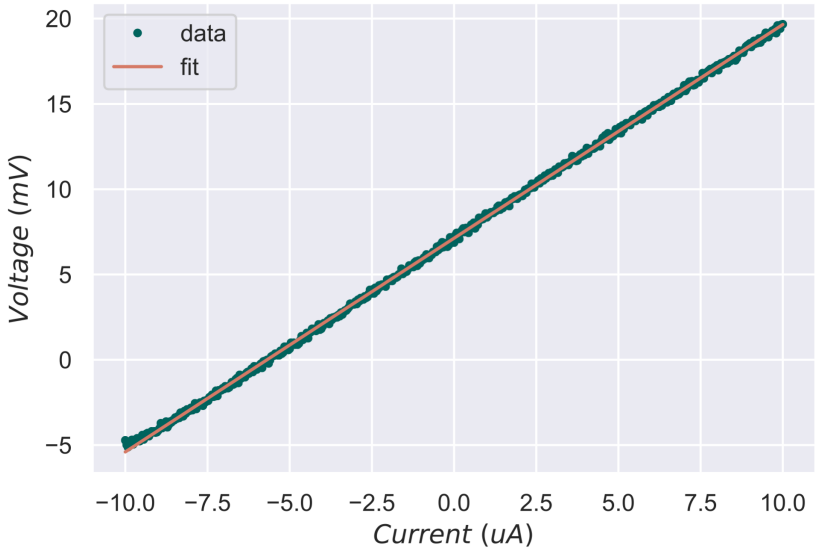

Figure 11: Data and fit results for the resistance measurement of the test22.

Figure 12 shows the penetration depth depending on the aluminium thickness, which is the final result we targeted for this project. As it can be seen, the tendency of both resonators measurement and resistance measurement is very similar. As the thickness increases the penetration depth decreases, which was the result expected. In 200 nm the penetration depth approaches the value for bulk aluminium. This might mean that we are already in the regime of type I superconductor. In this case, we should study the penetration depth with other formulas more appropriate for that regime. For example, studying the relation of the penetration depth with the temperature. Moreover, six chips is not enough data, so many more measurements should be performed. We also obtained the quality factor of the resonators for 100 nm, 75 nm and 25 nm thicknesses, which were $(1.27 \pm 0.26) \times 10^4$, $(1.37 \pm 0.45) \times 10^4$ and $(1.17 \pm 0.23) \times 10^4$, all of them in the expected range.

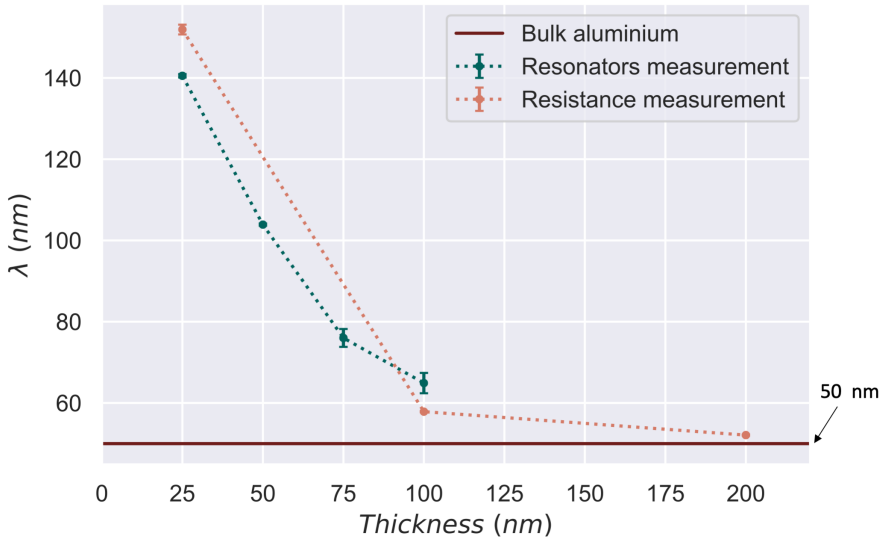

Figure 12: Penetration depth depending on the aluminium thickness for the resonators measurement and the resistance measurement.

6 Conclusions and future work

Several conclusion have already been done in terms of fabrication of thin film aluminium, micron size resonators. Some of them are that more chips with the first lift-off protocol should be fabricated. In

addition, using LOR3A generally improves the results. Moreover, the dimensions of the fabricated samples are different from the nominal design values. Also, another method should be tried to fabricate the small resonators like electron beam lithography as it has a lower resolution limit.

Furthermore, we needed to design and make a new mask that could be cleaned between different photolithographies. This new mask is already produced. I participated in the design which is in Figure 16a, 16b and 16c in the Annexes section. The chip with the resonators only contains three lines with five resonators. Then, it is easier to measure all the resonators of each line. In addition, only contains medium, large and distributed resonators. All of them could be measured in one run of the refrigerator using a switch. Moreover, the DC structures to measure the resistance are placed aside on a different chip. The DC structures include a 4-probe, a Hall bar and some Van der Pauw structures. There are also chips with three lines of small resonators. Some blank spaces are left in order to fabricate chips by e-beam.

On the other hand, for the measurement, we can conclude that the tendency observed in both ways (DC and resonators) to measure the penetration depth is the same. If the thickness increases the penetration depth decreases. Much more data is needed to be sure about the results obtained. The fitting performed in the resonators measurement works quite well. In addition, for the largest thicknesses, the penetration depth should be calculated with another method suited for that parameter regime. For example, using its dependence with the temperature. This must be done because in that case we might be in type I superconductor regime. The thickness in which aluminium passes from type II to type I should be then determined.

Furthermore, the material losses should be studied as they limit the performance of the qubits. It is important to know which type of loss mechanism is more relevant in each regime [13]. Moreover, the quality factors could be deeper studied. Finally, the penetration depth for other materials like granular aluminium could be studied.

A Annexes

Element	Part	Nominal dimensions (μm)	Fabrication dimensions (μm)
Launcher pad	Gap x	96	
	Gap y	96	
	Line x	192	
	Line y	160	
Line	Gap	6	
	Width	10	
DC meander	Spacing 0	65.5	
	Spacing 1	60.5	
	Line Gap	6	
	Line Width	10	
Test meander	Pad side	100	
	Pad diagonal	141	
	GND Gap	50	
	Line Width	2	
	Interline gap	5.5	
Large resonators	Line Distance	100	103.100±0.001
	Lateral Distance	175	
	Meander Width	6	5.895±0.001
	Meander Gap	6	4.895±0.001
	Finger Width	6	6.006±0.001
	Finger Gap	4	4.248±0.001
	Finger End Gap	4	4.395±0.001
	Meander Finger Distance	4	4.248±0.001
Medium resonators	Line Distance	40	35.160±0.001
	Lateral Distance	150	152.600±0.001
	Meander Width	4	4.248±0.001
	Meander Gap	4	3.662±0.001
	Finger Width	4	4.248±0.001
	Finger Gap	4	3.662±0.001
	Finger End Gap	4	3.662±0.001
	Meander Finger Distance	4	3.662±0.001
Small resonators	Line Distance	10	10.11±0.001
	Lateral Distance	200	
	Meander Width	2	2.051±0.001
	Meander Gap	2	1.758±0.001
	Finger Width	2	2.197±0.001
	Finger Gap	2	1.758±0.001
	Finger End Gap	4	3.809±0.001
	Meander Finger Distance	4	3.400±0.001
Distributed resonators	Line Distance	2	
	Width	10	
	Gap	6	
	Meander Distance	78	

Table 4: Nominal design values and dimensions after the fabrication from the test06 for large resonators, test24 for medium resonators and test10 for small resonators.

C:\Program Files (x86)\DaLEK\Recipes\20220128 _al_evap_with_no_descumming_dq_fz.prg

1	Sub Process	Root\Evap\Pocket 1\Ti 0.2nm/s	3min Tilt 0 Override DQ		0:00	0.0 nm
	0.00 °					
2	Sub Process	Root\Evap\wait recipe time	5:00	0.0 nm	0.00 °	
3	Sub Process	Root\Evap\Pocket 2-Al (liner)\Al (liner) 0.2nm/s x nmTilt 0 Planetary 1 rpm Override DQ 0:00				
	50.0 nm	0.00 °				
4	Sub Process	Root\Evap\wait recipe time	1:30	0.0 nm	0.00 °	

Subprocesses used

Root\Evap\Pocket 1\Ti 0.2nm/s 3min Tilt 0 Override DQ

1	LL Process	5.0e-07 mBar	120:00			Loadlock to process mode
2	Ch Process	7.0e-08 mBar	120:00			Chamber to process mode
3	Select crucible	Ti				Select E.B.G. crucible
material						
4	Wait	0:30				Wait for fixed time
5	Move planetary	Zero	0.0 °			Move planetary
6	Substrate Shutter	E.B.G.	Closed			Move the Substrate
Shutter						
7	Tilt substrate	Load	0.00 °			Tilt substrate table
8	E.B.G. Shutter	Open				Move the E.B.G. Source
Shutter						
9	E.B.G. Emission	80 mA	1:00			Ramp E.B.G. current
output						
10	Wait Ramp	E.B.G.				Wait for ramp(s) to
complete						
11	Wait	0:30				Wait for fixed time
12	Rate Control	0.20 nm/s	10:00			Start closed loop rate
control						
13	Wait	0:20				Wait for fixed time
14	Zero Thickness					Zero Xtal monitor
thickness						
15	Wait	3:00				Wait for fixed time
16	Substrate Shutter	E.B.G.	Closed			Move the Substrate
Shutter						
17	Wait	0:02				Wait for fixed time
18	E.B.G. Emission	0 mA	0:40			Ramp E.B.G. current
output						
19	Wait Ramp	E.B.G.				Wait for ramp(s) to
complete						
20	Wait	0:20				Wait for fixed time

Root\Evap\wait recipe time

1	Wait recipe time					Wait for time from recipe

Root\Evap\Pocket 2-Al (liner)\Al (liner) 0.2nm/s x nmTilt 0 Planetary 1 rpm Override DQ

1	LL Process	5.0e-07 mBar	120:00			Loadlock to process mode
2	Ch Process	7.0e-08 mBar	120:00			Chamber to process mode
3	Select crucible	Al (liner)				Select E.B.G. crucible
material						
4	Wait	0:30				Wait for fixed time
5	Rotate planetary	1.0 rpm				Rotate planetary
6	Tilt substrate	Evap	0.00 °			Tilt substrate table
7	Substrate Shutter	E.B.G.	Closed			Move the Substrate

Shutter						
8	E.B.G. Shutter	Open				Move the E.B.G. Source
Shutter						
9	E.B.G. Emission	200 mA	3:00			Ramp E.B.G. current
output						
10	Wait Ramp	E.B.G.				Wait for ramp(s) to
complete						
11	Wait	0:30				Wait for fixed time
12	Rate Control	0.20 nm/s	10:00			Start closed loop rate
control						
13	Wait	0:20				Wait for fixed time
14	Substrate Shutter	E.B.G.	Open			Move the Substrate
Shutter						
15	Zero Thickness					Zero Xtal monitor
thickness						
16	Wait recipe Thickness					Wait for thickness
from recipe						
17	Substrate Shutter	E.B.G.	Closed			Move the Substrate
Shutter						
18	Wait	0:02				Wait for fixed time
19	E.B.G. Emission	0 mA	0:40			Ramp E.B.G. current
output						
20	Wait Ramp	E.B.G.				Wait for ramp(s) to
complete						
21	Wait	0:20				Wait for fixed time

Figure 13: Aluminium evaporation recipe.

Chip	Photolitography			Evaporation			lift-off	
	Date	Place	LOR	Date	Place	Nom. Thick. (nm)	Date	Place
test01_100_SR	30/11/2021	CNM	No	30/11/2021	CNM	100	30/11/2021	CNM
test02_100_SR	30/11/2021	CNM	No	30/11/2021	CNM	100	30/11/2021	CNM
test03_100_SR	30/11/2021	CNM	No	30/11/2021	IFAE	100	1/12/2021	IFAE
test04_100_SR	30/11/2021	CNM	No	30/11/2021	IFAE	100	1/12/2021	IFAE
test05_100_SR	16/12/2021	CNM	No	16/12/2021	CNM	100	17/12/2021	CNM
test06_100_SR	16/12/2021	CNM	No	16/12/2021	CNM	100	17/12/2021	CNM
test07_100_SR	16/12/2021	CNM	No	17/12/2021	IFAE	100	17/12/2021	IFAE
test08_100_SR	16/12/2021	CNM	No	17/12/2021	IFAE	100	17/12/2021	CNM
test09_50_SR	02/02/2022	CNM	No	02/02/2022	IFAE	50	03/02/2022	CNM
test10_50_SR	02/02/2022	CNM	No	02/02/2022	IFAE	50	03/02/2022	CNM
test11_200_SR	02/02/2022	CNM	No	07/02/2022	IFAE	200	08/02/2022	CNM
test12_200_SR	02/02/2022	CNM	No	07/02/2022	IFAE	200	08/02/2022	CNM
test13_200_LOR	10/02/2022	CNM	Yes	10/02/2022	IFAE	200	11/02/2022	CNM
test14_200_LOR	10/02/2022	CNM	Yes	10/02/2022	IFAE	200	11/02/2022	CNM
test15_200_SR	10/02/2022	CNM	No	10/02/2022	IFAE	200	11/02/2022	CNM
test16_200_SR	10/02/2022	CNM	No	10/02/2022	IFAE	200	11/02/2022	CNM
test17_150_LOR	17/02/2022	CNM	Yes	17/02/2022	IFAE	150	18/02/2022	CNM
test18_150_LOR	17/02/2022	CNM	Yes	17/02/2022	IFAE	150	18/02/2022	CNM
test19_75_LOR	15/02/2022	CNM	Yes	15/02/2022	IFAE	75	16/02/2022	CNM
test20_75_LOR	15/02/2022	CNM	Yes	15/02/2022	IFAE	75	16/02/2022	CNM
test21_25_LOR	15/02/2022	CNM	Yes	15/02/2022	IFAE	25	16/02/2022	CNM
test22_25_LOR	15/02/2022	CNM	Yes	15/02/2022	IFAE	25	16/02/2022	CNM
test23_200_LOR	17/02/2022	CNM	Yes	18/02/2022	CNM	200	18/02/2022	CNM
test24_200_LOR	17/02/2022	CNM	Yes	18/02/2022	CNM	200	18/02/2022	CNM
test25_150_LOR	8/03/2022	CNM	Yes	8/03/2022	IFAE	150	9/03/2022	CNM
test26_150_LOR	8/03/2022	CNM	Yes	8/03/2022	IFAE	150	9/03/2022	CNM
test27_150_LOR	8/03/2022	CNM	Yes	8/03/2022	IFAE	150	9/03/2022	CNM

Table 5: Chip characteristics.

Chip	Resonator type	Launchers	Resonators	Meander	Lines
test01_100_SR	LR	G	10 G	G	G
	MR	G	1 B, 9 G	G, particle	G
	SR	G	10 G	G	G
	DR	G	10 G, particles	G	G, Al particle
test02_100_SR	LR	G	10 G	G	9 G, 1 BLO
	MR	G	10 B	G	G
	SR	G	10 B	B, spots & BLO	B
	DR	G	10 B, spots	B,spots	G
test03_100_SR	LR	G	8 G, 2 BLO & spots	Spot	G, B meander line
	MR	G	1 G, 9 BLO	G	B resonators line
	SR	G	10 BLO & spots	G	G
	DR	2 BLO	3 BLO, 7 G	G	B resonators line
test04_100_SR	LR	2 BLO	10 B	BLO	BLO
	MR	3 G, 3 BLO	10 BLO	BLO	BLO
	SR	4 BLO	10 BLO	BLO	BLO
	DR	3 G, 3 BLO	10 BLO	BLO	BLO
test05_100_SR	LR	G	6 G, 4 spots	G	G
	MR	G	10 G	G	G
	SR	G	2 G	G	G
	DR	G	1 B, 9 G	B, spots short	G
test06_100_SR	LR	G	2 B	G	G
	MR	G	8 G, 2 B, particle & short	G	G
	SR	G	10 G, particle	G	G
	DR	G	10 G, particle	G	G
test07_100_SR	LR	2 G, 4 BLO	3 G, 7 BLO	BLO	BLO meander lines
	MR	G	6 G, 4 BLO	G	G
	SR	BLO	10 BLO	BLO	BLO
	DR	3 G, 3 BLO	10 BLO	BLO	BLO
test08_100_SR	LR	G	10 G	G	G
	MR	G	10 G	Al particle	G
	SR	G	1 B, 9 G	G	G
	DR	G	10 G	Al particle	G
test09_50_SR	LR	1 B	10 G	B	G
	MR	G	10 G, particle	G	G
	SR	G	2 G, 8 B, BLO & particle	G	G
	DR	G	9 G, 1 B,	G	G
test10_50_SR	LR	G	9G, 1 B	G	G
	MR	G	10 G	G	G
	SR	G	10 BLO	G	G
	DR	G	7 G, 3 B, particle	G	G
test11_200_SR	LR MR SR DR	BLO	10 BLO	BLO	BLO
test12_200_SR	LR MR SR DR	BLO	10 BLO	BLO	BLO
test13_200_LOR	LR MR SR DR	BLO	10 BLO	BLO	BLO
test14_200_LOR	LR MR SR DR	BLO	10 BLO	BLO	BLO

Chip	Resonator type	Launchers	Resonators	Meander	Lines
test15_200_SR	LR MR SR DR	BLO	10 BLO	BLO	BLO
test16_200_SR	LR MR SR DR	BLO	10 BLO	BLO	BLO
test17_200_LOR	LR MR SR DR	G G G G	9 G, 1 B 8 G, 2 BLO 10 B 9 G, 1 B	B, scratch G G B, scratch	G Particles G G
test18_200_LOR	LR MR SR DR	G 1 B, 5 G G 1 B, 5 G	6 G, 4 BLO 1 G, 9 BLO 10 B 7 G, 3 B	G B BLO G	G G G G
test19_75_LOR	LR MR SR DR	G G G G	10 G, particles 10 G, particles 10 BLO 10 G	G Al particle Particle G	Particle Particles G B meander line
test20_75_LOR	LR MR SR DR	G G G G	10 G, particles 10 G, particle 10 BLO 10 G	G G G G	G G G G
test21_25_LOR	LR MR SR DR	G G 1 BLO, 5 G G	1 G, 9 BLO 6 G, 4 B, particles 10 BLO 10 G	G G BLO G	Particle B resonators line G Particles
test22_25_LOR	LR MR SR DR	G 1 B, 5 G G G	7 G, 3 BLO 10 G 10 BLO 2 G, 8 BLO	G G G G	G G G G
test23_200_LOR	LR MR SR DR	G G G G	4 G, 6 BLO 7 BLO, 3 G 10 B 3 G, 7 B	G G G G	G G G BLO
test24_200_LOR	LR MR SR DR	3 B, 3 G G G G	7 G, 3 BLO 5 BLO, 5 G 10 B 3 G, 7 B	G G G G	G G G Meander lines scratch
test25_150_LOR	LR MR SR DR	G G G G	8 G, 2 B 1 B, 9 G 10 B 10 G	G Al particles G Al particles	G G G G
test26_150_LOR	LR MR SR DR	G 4 G, 2 B, scratch 5 G,1 B G	6 B, 4 G 8 G, 2 B, scratch 10 B 5 G, 5 B, scratch	BLO G B G	B G B Scratch
test27_150_LOR	LR MR SR DR	G 5 G, 1 B G G	8 G, 2 B 9 G, 1 B 10 B 10 G	G G B G	Scratch G G G

Table 6: Chip results characterization. BLO: Bad lift-off, G: Good, B: Bad.

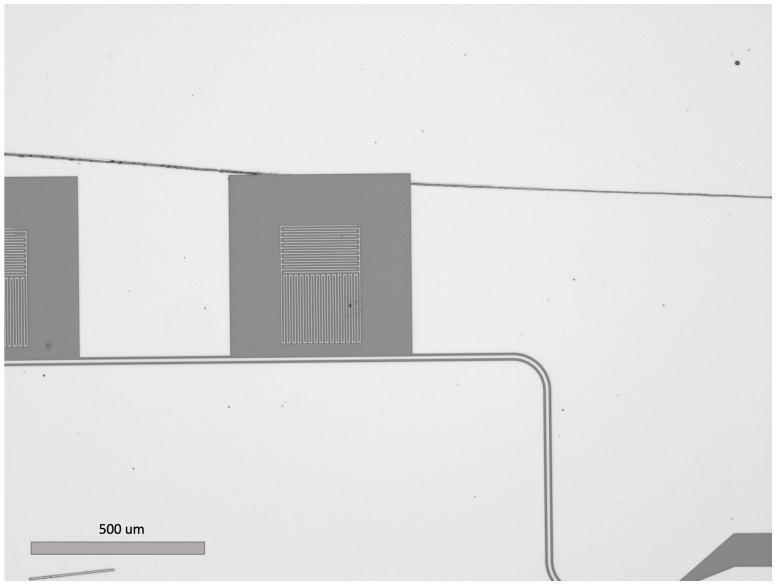

Figure 14: Image after the dicing of the medium resonators from test06.

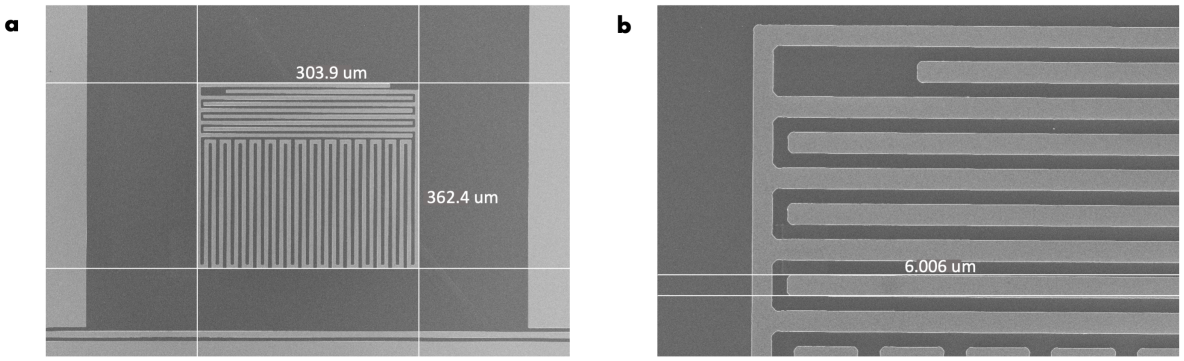

Figure 15: Pictures of a large resonator from test06 done by a scanning electron microscope (SEM). From these pictures some dimensions of the fabricated samples were extracted. **a.** The dimensions of the whole resonator. **b.** The dimension of a finger's width.

Nominal Al thickness (nm)	f_{res} (GHz)	f_{sim} (GHz)	C (fF)	L_{sim} (nH)	L_{total} (nH)	L_{kin} (pH)	λ (nm)
25	5.157	7.028	287.526	1.783	3.313	1529.605	781.166
	5.193	7.130	279.413		3.362	1578.686	806.232
	5.262	7.181	275.397		3.322	1538.851	785.888
	5.267	7.232	271.579		3.362	1579.156	806.472
	5.336	7.286	267.531		3.325	1542.326	787.663
	5.372	7.338	263.746		3.328	1544.996	789.026
	5.437	7.391	259.970		3.296	1513.087	772.730
50	6.285	6.978	291.686	1.783	2.198	415.440	212.164
	6.332	7.088	287.526		2.197	414.194	211.528
	6.373	7.078	283.502		2.200	416.868	212.894
	6.422	7.130	279.413		2.198	415.129	212.006
	6.452	7.181	275.397		2.209	426.495	217.810
	6.493	7.232	271.579		2.212	429.349	219.268
	6.545	7.286	267.531		2.210	427.006	218.071
	6.584	7.338	263.746		2.215	432.382	220.817
	6.651	7.391	259.970		2.203	419.772	214.377
	6.711	7.475	254.201		2.213	429.791	219.494
75	7.272	7.460	252.594	1.801	1.896	95.313	48.676
	7.278	7.540	247.262		1.934	133.009	67.928
	7.291	7.580	244.659		1.948	146.620	74.879
	7.312	7.610	242.734		1.952	150.807	77.017
	7.326	7.650	240.202		1.965	163.848	83.677
	7.357	7.680	238.330		1.964	162.636	83.058
	7.377	7.710	236.478		1.968	167.290	85.435
	7.409	7.750	234.043		1.972	170.625	87.137
100	7.005	7.160	218.716	2.259	2.360	101.171	51.668
	7.031	7.220	215.100		2.382	123.176	62.906
	7.110	7.280	211.565		2.368	109.412	55.876
	7.126	7.350	207.554		2.403	144.348	73.718
	7.198	7.405	204.483		2.391	131.893	67.357
	7.210	7.455	201.749		2.415	156.230	79.786
	7.000	7.500	199.335		2.391	132.119	67.473
	7.407	7.575	195.408		2.363	103.730	52.975
	7.435	7.665	190.846		2.401	142.021	72.530

Table 7: Resonators measurement values.

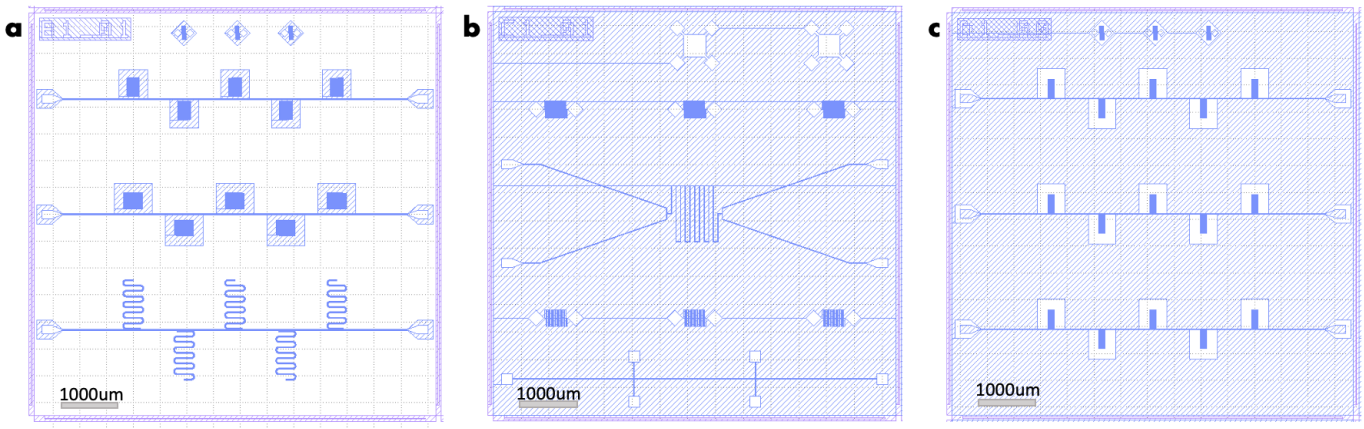

Figure 16: Design of the mask for the next generation of chips. **a.** Three lines with medium, large and distributed resonators. **b.** Different structures for the DC measurements. **c.** Three lines with small resonators.

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